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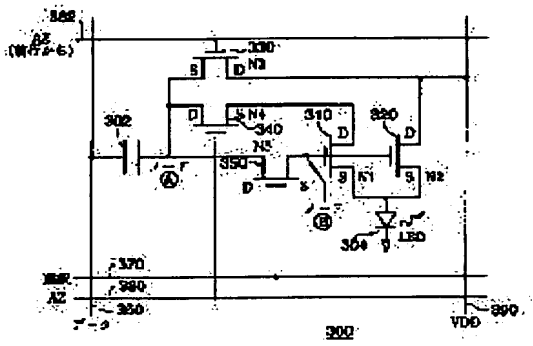
(54) ACTIVE MATRIX LIGHT EMITTING DIODE PICTURE ELEMENT STRUCTURE AND METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce uneveness of a current in a light emitting diode(LED) so as to improve uniformity of luminance by composing picture element structure of NMOS transistors, a capacitor and the LED.
SOLUTION: Picture element structure 300 is composed of five NMOS transistors 310-350, a capacitor 302 and an LED 304. A selection line 370 is connected to a gate of the transistor 350, and a data line 360 is connected to one terminal of the capacitor 302. An auto-zero line 380 is connected to a gate of the transistor 340, and a VDD line 390 is connected to the drains of the transistors 320, 220. One terminal of the capacitor 302 is connected to the source of the transistor 330 and the drains of the transistors 340, 350, and the sources of the transistors 310, 320 are connected to one terminal of the LED 304. With this constitution, unevenness of a current can be reduced in the LED 304.



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CLAIMS

[Claim(s)]
[Claim 1] It is a display equipped with at least one pixel. The pixel concerned (1) The 1st transistor which has the gate which is an object for the connection to 1st selection Rhine, the source, and a drain, (2) The 1st terminal to which the drain of the 1st transistor concerned is connected, The capacitor which has the 2nd terminal, and the gate which is an object for the connection to (3) auto-zero line, The 2nd transistor which has the drain with which the drain concerned of the 1st transistor concerned is connected with the source, (4) The gate which is an object for the connection to 2nd selection Rhine, and the source connected to the drain of the 2nd transistor concerned, the 3rd transistor which has a drain, and (5) -- with the gate connected to the source of the 1st transistor concerned The 4th transistor which has the drain connected to the source and the source concerned of the 2nd transistor concerned, (6) The gate connected to the source of the 1st transistor concerned, and the source, The 5th transistor which has the drain connected to the drain concerned of the 3rd transistor concerned, (7) Display characterized by the source of the 4th transistor concerned and the source of the 5th transistor concerned consisting of the optical element which has two terminals connected to one terminal.
[Claim 2] The display according to claim 1 said whose optical element is an organic light emitting diode (OLED).
[Claim 3] The display according to claim 1 or 2 said each transistor of whose is a thin film transistor built with amorphous silicon.
[Claim 4] A display given in any of claims 1-3 said whose 2nd selection Rhine is auto-zero lines from the previous line they are.
[Claim 5] It is the display equipped with at least one pixel. The pixel concerned (1) The 1st transistor which has the gate which is an object for the connection to one selection Rhine, the source, and a drain, (2) The 1st terminal to which the drain of the 1st transistor concerned is connected, The capacitor which has the 2nd terminal, and the gate which is an object for the connection to (3) auto-zero line, The 2nd transistor which has the drain with which the drain concerned of the 1st transistor concerned is connected with the source, (4) Diode which has the 1st terminal connected to the source of the 2nd transistor concerned, and the 2nd terminal for connection with lighting Rhine, (5) The gate connected to the source of the 1st transistor, and the source, the 3rd transistor which has the drain connected to the 1st terminal of the diode concerned, and (6) -- the display characterized by the source of the 3rd transistor concerned consisting of the optical element which has two terminals connected to one terminal.
[Claim 6] The display according to claim 5 said whose diode is schottky diode.
[Claim 7] It is the display equipped with at least one pixel. The pixel concerned (1) The 1st transistor which has the gate which is an object for the connection to 1st selection Rhine, the source, and a drain, (2) The 1st terminal to which the drain of the 1st transistor concerned is connected, The capacitor which has the 2nd terminal, and the gate which is an object for the connection to (3) auto-zero line, The 2nd transistor which has the source to which the source concerned of the 1st transistor concerned is connected, and a drain, (4) The gate which is an object for the connection to 2nd selection Rhine, and the source connected to the drain of the 2nd transistor concerned, the 3rd transistor which has a drain, and (5) -- with the gate connected to the source of the 1st transistor concerned The 4th transistor which has the drain connected to the source and the above-mentioned source of the 3rd transistor concerned, (6) The gate connected to the source of the 1st transistor concerned, and the source, The 5th transistor which has the drain connected to the drain concerned of the 3rd transistor concerned, (7) Display characterized by the source of the 4th transistor concerned and the source of the 5th transistor concerned consisting of the optical element which has two terminals connected to one terminal.

[Claim 8] The display according to claim 7 said whose optical element is an organic light emitting diode (OLED).
[Claim 9] The display according to claim 7 or 8 said whose 2nd selection Rhine is an auto-zero line from the previous line.
[Claim 10] (1) at least one auto-zero-ized pixel structure, and (2) -- the display which consists of the auto-zero line connected to the auto-zero-ized pixel structure concerned in order to enable activation of auto-zero-izing at the auto-zero-ized pixel structure concerned, and the 2nd line connected to the auto-zero-ized pixel structure concerned so that one electrical potential difference might be carried to the auto-zero-ized pixel structure concerned, in order to extend the range of (3) auto-zero electrical potential differences.
[Claim 11] The approach which is the approach of turning on the display which has at least one pixel including the circuit which controls the impression energy to an optical element, and is characterized by to consist of the step which auto-zero-izes the (a) pixel, the step which loads data to the pixel concerned via (b) data line, and the step which turns on the optical element concerned based on the data by which (c) preservation was carried out.
[Claim 12] The approach according to claim 11 of containing further the step which precharges said pixel before said auto-zero-ized step (a).
[Claim 13] The approach according to claim 11 or 12 said auto-zero-ized step (a) contains the step which impresses criteria black level.
[Claim 14] The approach which is the approach of turning on the display which has at least one pixel, and is characterized by to consist of the step which adjusts input pixel data based on the pixel parameter by which (a) (b) measurement was carried out with the step which measures the pixel parameter of the pixel concerned, and the step which turns on the pixel concerned based on the input pixel data by which (c) adjustment was carried out.
[Claim 15] The approach according to claim 14 said measurement step (a) measures externally the current pulled out by said pixel.
[Claim 16] The approach according to claim 14 or 15 said adjustment step (b) amends said pixel data using said measured pixel parameter in order to ask for an electrical-potential-difference offset (Voffset) parameter.
[Claim 17] The approach according to claim 16 said adjustment step (b) amends said pixel data further using said measured pixel parameter in order to ask for a gain factor (C) parameter.
[Claim 18] It is the system which consists of the display which changes from two or more pixels to ** when it connects with a display controller and the display controller concerned. Each pixel concerned The gate for connection to (1) 1st selection Rhine, the source and the 1st transistor which consists of a drain, and (2) -- with the 1st terminal connected to the drain concerned of the 1st transistor concerned The capacitor which has the 2nd terminal, and the gate for connection to (3) auto-zero line, The 2nd transistor which has the source connected to the source concerned of the 1st transistor concerned, and a drain, (4) The gate for connection to 2nd selection Rhine, and the source connected to the drain concerned of the 2nd transistor concerned, the 3rd transistor which has a drain, and (5) -- with the gate connected to the source concerned of the 1st transistor concerned The 4th transistor which has the drain connected to the source and the source concerned of the 3rd transistor concerned, (6) The gate connected to the source concerned of the 1st transistor concerned, and the source, the 5th transistor which has the drain connected to the drain concerned of the 3rd transistor concerned, and (7) -- the system characterized by the source of the 4th transistor concerned and the source of the 5th transistor concerned consisting of the optical element which has two terminals connected to one terminal.
[Claim 19] (1) the measurement module for measuring the pixel parameter of a pixel, and (2) -- the display controller who has a store for saving the measured pixel parameter concerned, and (3) -- the system which consists of the display connected to the display controller concerned in order to display the input pixel data adjusted based on the saved pixel parameter concerned.
[Claim 20] The system according to claim 19 which has a current detecting circuit for said measurement module to measure the current pulled out by said pixel.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to active-matrix light emitting diode pixel (pixel) structure. This invention relates to the actuation approach of the pixel structure of reducing the heterogeneity of a current in the light emitting diode of pixel structure, and improving the homogeneity of brightness in detail, and said active-matrix light emitting diode pixel structure. In addition, this application is the U.S. ******** of September 29, 1997 application. 060 60/386 Number and U.S. ******** of September 29, 1997 application 060 60/387 If the priority of a number is asserted, to **, it will quote at this application.
[0002]
[Description of the Prior Art] The matrix display which turns on a pixel using matrix addressing as shown in drawing 1 is common knowledge in the technical field concerned. The typical display 100 has, the screen element (pixel) 160, i.e., the display element, constituted by the row and column. This display contains the string data generator 110 and the line data generator 120. While sequential energization of each line is carried out through line Rhine 130 in actuation, the pixel which corresponds using corresponding train Rhine energizes. In a passive matrix display, although one pixel of each line is turned on at a time one by one, in an active matrix display, data are loaded to the pixel of each train one by one. That is, although "each train of a passive matrix display is only in an energization condition in a part of all mere frame time", what each train of an active matrix display "is made into an energization condition for" over the whole frame time is made.
[0003] Various play techniques (LCD), for example, a liquid crystal display, and a light emitting diode display (LED) came to be used with spread of a portable display, for example, a laptop computer. It is important to save the power of the portable system which uses a display in a portable display generally, and to enable it to extend the "time" of a portable system by it.
[0004] In LCD, the back light is turned on over the whole term of a display in use. That is, in order to turn on all the pixels in LCD and to make a certain pixel "dark", the light which passes along a pixel is interrupted in a polarization layer. On the other hand, a LED display abolishes the need of only the energized pixel being turned on and turning on a dark pixel, and is planning power saving.
[0005] The active-matrix LED pixel structure 200 of the conventional technique of having two NMOS transistors N1 and N2 in drawing 2 is shown. In this pixel structure, by energizing to a transistor N1, data (electrical potential difference) are first saved to Capacitor C, then, it energizes to the "drive transistor" N 2, and LED is turned on. Although electricity can be saved also for the display which used the pixel structure 200, with this pixel structure, an uneven intensity level is presented according to some causes.
[0006] In the first place, it is observed that the brightness of LED is proportional to the current passing through that. During use, since the threshold voltage of the "drive transistor" N 2 carries out a drift, the current which passes along LED may change. Change of this current serves as a cause of the heterogeneity of the brightness of a display.
[0007] Another cause of the heterogeneity of the brightness of a display can be found [second] out in manufacture of the "drive transistor" N 2. In some cases, homogeneous reservation of the initial threshold voltage of a transistor is made from a difficult ingredient, consequently the "drive transistor" N 2 is changed for every pixel.
[0008] The electrical parameter of LED may also present [third] heterogeneity. For example, under bias temperature stress conditions, the increment in the turn-on electrical potential difference of OLED (organic light emitting diode) is expected.
[0009] Therefore, the pixel structure of reducing the heterogeneity of the current resulting from fluctuation

of the threshold voltage in the "drive transistor" of pixel structure, and the approach relevant to it are needed in the technical field concerned.
[0010]
[Problem(s) to be Solved by the Invention] This invention aims at offering the LED (or OLED) pixel structure of improving the homogeneity of brightness by reduction of the heterogeneity of the current in the light emitting diode of pixel structure, and an approach.
[0011]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention persons came to complete a header and this invention for the ability of five NMOS transistors, a capacitor, and the pixel structure that consists of LED to solve the above-mentioned technical problem, as a result of inquiring wholeheartedly.
[0012] The first summary of this invention is a display equipped with at least one pixel. Namely, the pixel concerned (1) The 1st transistor which has the gate which is an object for the connection to 1st selection Rhine, the source, and a drain, (2) The 1st terminal to which the drain of the 1st transistor concerned is connected, The capacitor which has the 2nd terminal, and the gate which is an object for the connection to (3) auto-zero line, The 2nd transistor which has the drain with which the drain concerned of the 1st transistor concerned is connected with the source, (4) The gate which is an object for the connection to 2nd selection Rhine, and the source connected to the drain of the 2nd transistor concerned, the 3rd transistor which has a drain, and (5) -- with the gate connected to the source of the 1st transistor concerned The 4th transistor which has the drain connected to the source and the source concerned of the 2nd transistor concerned, (6) The gate connected to the source of the 1st transistor concerned, and the source, The 5th transistor which has the drain connected to the drain concerned of the 3rd transistor concerned, (7) The source of the 4th transistor concerned and the source of the 5th transistor concerned consist in the display characterized by consisting of the optical element which has two terminals connected to one terminal.
[0013] In the desirable mode of the 1st summary, pixel structure consists of three transistors and one diode.
[0014] In other desirable modes of the 1st summary, pixel structure is different pixel structure of having five transistors.
[0015] Pixel structure is equipped with one Rhine of the addition which extends the auto-zero-ized electrical-potential-difference range in other desirable modes of the 1st summary.
[0016] The 2nd summary of this invention measures a pixel parameter, and consists in one external measurement module which adjusts input pixel data using it, and various measuring methods.
[0017]
[Embodiment of the Invention] Hereafter, this invention is explained in detail using a drawing. In addition, in order to make an understanding easy, the element common to each drawing attached the same possible sign.
[0018] Drawing 3 is the schematic drawing of the active-matrix LED pixel structure 300 by this invention. In a desirable embodiment, active-matrix LED pixel structure is carried out using the transistor made using the thin film transistor (TFT), i.e., polish recon, or the amorphous silicon. Similarly, organic light emitting diode (OLED) is used for active-matrix LED pixel structure in a desirable embodiment. Although this pixel structure is carried out using a thin film transistor and an organic light emitting diode, even if this invention uses other transistors and light emitting diodes of a type, it can be carried out.
[0019] This pixel structure 300 offers a uniform current drive, even when [that the heterogeneity of transistor threshold voltage (Vt) is large and] the heterogeneity of an OLED turn-on electrical potential difference is large. That is, it is desirable to maintain at homogeneity the current which passes along OLED, and to secure the homogeneity of the brightness of a display by it.
[0020] When drawing 3 is referred to, the pixel structure 300 consists of five NMOS transistors N1 (310), N2 (320), N3 (330), N4 (340), and N5 (350), a capacitor 302, and LED (OLED) (optical element)304 (optical element). Selection Rhine 370 is connected to the gate of a transistor 350. The data line 360 is connected to one terminal of a capacitor 302. The auto-zero line 380 is connected to the gate of a transistor 340. VDD Rhine 390 is connected to the drain of transistors 320 and 330. The auto-zero line 382 from the continued line in a pixel array is connected to the gate of a transistor 330.
[0021] It should note being able to carry out the auto-zero line 382 from the previous line as 2nd selection Rhine. That is, the timing of a current pixel can be used without the auto-zero line 382 from the previous line needing the 2nd selection Rhine, and reduces the current complexity and the cost of a pixel by it.
[0022] One terminal of a capacitor 302 is connected to the source of a transistor (setting to Node A) 330, and the drain of transistors 340 and 350. The source of a transistor 350 is connected to the gate of transistors

(setting to Node B) 310 and 320. The drain of a transistor 310 is connected to the source of a transistor 340. Finally, the source of transistors 310 and 320 is connected to one terminal of LED304.
[0023] As mentioned above, the drive of an organic LED display has many problems by various heterogeneity. This invention relates to the structure of the organic LED display for these problems. That is, each LED pixel is driven by the insensible approach to fluctuation of an LED turn-on electrical potential difference, or fluctuation of TFT threshold voltage. That is, the auto-zero-ized approach used in order to cope with fluctuation of an LED turn-on electrical potential difference or TFT threshold voltage can be used for the present pixel, and it can ask for an offset voltage parameter.
[0024] Furthermore, data are supplied to each pixel as a data electrical potential difference by the approach extremely similar to the approach used in the conventional active-matrix liquid crystal display. Consequently, external or built-in can also be used for the display structure of this invention to the scanner of the conventional row and column.
[0025] Five TFT(s), one capacitor, and LED are used for the pixel of this invention. Connection of TFT is not at the cathode of LED, it should note connecting with an anode and this is needed by the fact that ITO is a hole emitter in organic [conventional / LED]. Therefore, LED is not at the drain of TFT and is connected to the source. The train of each display has two line Rhine (an auto-zero line and selection Rhine), and 1-1 / 2 train Rhine (a data line and +VDD Rhine shared with the next train). The wave on each Rhine is also shown in drawing 4 . Actuation of a pixel 300 is explained in full detail in three phase, i.e., a three-stage, below.
[0026] The first phase is a precharge phase. The forward pulse on auto-zero (AZ) Rhine of the previous line 382 turns "ON" a transistor 330, and precharges the node A of a pixel to Vdd, +10V [for example,]. Next, in order that a data line may write data in the pixel of the previous line, it changes from the base-line value, and returns to the base line. This does not have the net effectiveness to a pixel under consideration.
[0027] The second phase is an auto-zero phase. current AZ Rhine and current SELECT Rhine of a line -- high -- becoming -- transistors 340 and 350 -- "ON" -- carrying out -- transistor N1 The gate of 310 is dropped, an auto-bias is applied to a turn-on electrical potential difference, and a pole hoe ****** current is passed to LED. In this phase, the sum total of the turn-on electrical potential difference of LED and the threshold voltage of N1 is saved at the gate of N1. Since N1 and N2 approach very much and they can be arranged, those initial threshold voltage is extremely similar. Furthermore, the gate voltage Vgs to the source of these two transistors is the same ****. Since it depends for the drift of the threshold voltage of TFT only on Vgs over all the lives of TFT, it can be considered that the threshold voltage of these devices is followed over all the lives of TFT. Therefore, the threshold voltage of N2 is also saved on the gate. After completion of auto-zero-izing, while an auto-zero line returns to a low (low), selection Rhine is still yes (high).
[0028] The third phase is a data write-in phase. Data are impressed as an electrical potential difference exceeding a base-line electrical potential difference to a data line, and are written in a pixel through a capacitor. Next, selection Rhine is related with a low, the sum total of return, a data electrical potential difference, a plus LED turn-on electrical potential difference, and the threshold voltage of plus N2 is related with the remaining frames, and it is saved at Node B. It should note being able to use the capacitor from Node B to +Vdd so that the saved data may not be lost by leak.
[0029] In short, a thin current (trickle current) is used during an auto-zero phase, and the turn-on electrical potential difference of LED and threshold voltage of N2 "are measured", and are saved at Node B. This auto-zero phase is essentially actuation in the current drive mode in which a drive current is very small. An increment is given to LED using the data electrical potential difference impressed only after became a write-in phase after an auto-zero phase. Therefore, it can be said that this invention has "a hybrid drive" rather than an electrical-potential-difference drive or a current drive. The hybrid drive approach does not have a fault in an electrical-potential-difference drive and a current drive, and combines both advantage. Fluctuation of the turn-on electrical potential difference of LED and the threshold voltage of TFT is amended completely like the case in a current drive. Since all Rhine on a display is driven with an electrical potential difference to coincidence, it can drive at high speed.
[0030] attention **** -- the increment of the data electrical potential difference impressed to things at a data line 360 is divided between Vgs(es) of N2 (320) and LED rather than appears directly over the LED304 whole. This only means that there is non-line [from a data electrical potential difference to an LED electrical potential difference] type mapping. Although this mapping is combined with non-line [from an LED electrical potential difference to an LED current] type mapping and the transfer function of a data electrical potential difference to the whole LED electrical potential difference is generated, this is

monotonous and stable over all the lives of a display as mentioned above.
[0031] The transistor (N3, N4, and N5) in the pixel by which a threshold is not amended of the advantage of the present pixel structure 300 is [only 1 train time amount] that it is expected that it does not shift to the forge fire which a duty cycle is very short and can be recognized since it becomes ON per frame. Furthermore, N2 is the only transistor in the present pass of LED. If the transistor by which the series connection was carried out on this pass may degrade display effectiveness, or may generate the problem by non-amended TFT threshold shift and is shared by all the pixels on one train, it may bring about the remarkable cross talk of a lengthwise direction.
[0032] A selection pulse and an auto-zero (AZ) pulse are formed with a line scanner. In addition to a fixed base-line electrical potential difference (arbitration), string data is impressed in the time slot between AZ pulses. On a data line, the downward edge of a selection signal is generated, while data are effective. External [of either a direct sample type or a chopped lamp type / various kinds of] or a built-in train scanner can generate data by this timing.
[0033] According to the above-mentioned pixel structure, a large-sized accepting-reality display can be built using organic [LED]. or [of course, / that a display element or the turn-on electrical potential difference of TFT shifts current pixel structure also to the display technique of the arbitration which uses the display element which needs a drive current especially] -- or when uneven, it can apply.
[0034] Drawing 5 is the schematic drawing of the desirable embodiment of the active-matrix LED pixel structure 500 by this invention. Although this pixel structure 500 is similar to the pixel structure 300 of drawing 3 , one schottky diode is being used for it instead of two transistors here.
[0035] Using five transistors per pixel is mentioned as one of the faults which the pixel structure 300 may have. That is, since many transistors are used for each pixel, the fill factor (fill factor) (assuming the bottom side emission which passes along an active plate) of a pixel, and its yield (yield) may also be affected. Therefore, the pixel structure 300 achieves the same function as the above, reducing a transistor count from five pieces to each pixel at three pieces only using one schottky diode.
[0036] In drawing 5 , a pixel 500 consists of the schottky diode 540 of 502 or 1 capacitor of three NMOS transistors [3 (530) or 1] N1 (510), N2 (520), and N, and LED (OLED)550 (optical element). Selection Rhine 570 is connected to the gate of a transistor 530. The data line 560 is connected to one terminal of a capacitor 502. The auto-zero line 580 is connected to the gate of a transistor 520. Lighting Rhine (similar to VDD Rhine) 590 is connected to one terminal of schottky diode 540.
[0037] One terminal of a capacitor 502 is connected to the drain of transistors (setting to Node A) 520 and 530. The source of a transistor 530 is connected to the gate of a transistor (setting to Node B) 510. The drain of a transistor 510 is connected to the source of a transistor 520, and one terminal of schottky diode 540.
[0038] The pixel structure 500 also operates as follows in 3 of a precharge phase, an auto-zero phase, and a data write-in phase phases. Before all lighting Rhine is mutually combined around the display and a precharge phase starts, these lighting Rhine is held at the electrical potential difference VILL of plus of abbreviation +15V. In the following explanation, a line under consideration is called "Line i." The wave on each Rhine is also shown in drawing 6 .
[0039] The first phase is a precharge phase. Precharge will be started, if auto-zero (AZ) Rhine turns ON a transistor N2 and selection Rhine turns ON a transistor N3. This phase is performed when a data line is in reset level. Although the electrical potential difference in Nodes A and B rises to the same electrical potential difference as the drain of a transistor N1, this is a diode descent lower than VILL.
[0040] The second phase is an auto-zero phase. Next, lighting Rhine falls to a ground. all the pixels in this phase and on an array -- a short time -- it becomes dark. Here, schottky diode 540 insulates the drain of a transistor N1 from grounded lighting Rhine, and auto-zero-ization of N1 starts. If Node B reaches an electrical potential difference almost equal to the turn-on electrical potential difference of the threshold voltage plus LED 550 of a transistor N1, a transistor N2 will be turned "OFF" using AZ Rhine, and lighting Rhine will return to VILL. All the pixels of the line which was not chosen light up again.
[0041] The third phase is a data write-in phase. Next, the data about Line i are impressed to a data line. The power surge in Nodes A and B makes equal the difference between the reset voltage level of a data line, and a data voltage level. Thus, fluctuation of the threshold voltage of a transistor N1 and the turn-on electrical potential difference of LED is amended. After the electrical potential difference in Node B settles down, a transistor N3 is turned OFF using selection Rhine about Line i, and a data line is reset. A data electrical potential difference suitable to the following frame is saved now at a pixel.
[0042] In the above, although it had the advantage of 5 transistor pixel described previously, 3 transistor pixel for an OLED display with few transistor counts was explained. It is that a separate transistor is used

for auto-zero-izing and an LED drive by 5 transistor pixel as further advantage. In order for a pixel 300 to operate appropriately, it is required for the initial threshold of these two transistors to be in agreement, and to carry out a drift similarly over the whole term of a life. According to the place which the latest experimental data suggests, if the drain electrical potential differences of TFT(s) (they are these transistors like) differ mutually, similarly the drift of both the TFT(s) will not be carried out. Therefore, a pixel 500 performs auto-zero-ization on the same transistor which drives LED so that suitable auto-zero-ization may be guaranteed.

[0043] Drawing 7 is the schematic drawing of the alternative embodiment of the active-matrix LED pixel structure 700 by this invention. Although this pixel structure 700 is similar to the pixel structure 300 of drawing 3 , it generates a still more exact auto-zero electrical potential difference.

[0044] That is, in drawing 3 , each precharge cycle produces auto-zero-ization from the fact of pouring the big plus charge QPC into the node A of a pixel 300 as shown in drawing 3 . The capacitance of all in a precharge phase and on Node A is almost from Capacitor Cdata, and the charge poured into Node A is expressed with a formula (1).

[0045]

[Equation 1]

$$Q_{pc} \cong C_{data}(V_{DD} - V_A) \qquad (1)$$

[0046] VA is an electrical potential difference in the node A before a precharge phase starts here. VA is influenced by the data beforehand given to the pixel 300, the threshold voltage of N3 (300), and the turn-on electrical potential difference of LED304. Since Cdata is big capacitance (about 1pF), QPC is also as large as 10 picocoulomb (picocoulomb) extent.

[0047] When it is in the auto-zero level by which the pixel 300 was stabilized, QPC flows through N1 (300) and LED304 during an auto-zero phase. Since auto-zero spacing (interval) is short (about 10microsec), a gate pair source auto-zero electrical potential difference higher than the threshold voltage may remain in N1, and LED exceeds and auto-zero-izes the turn-on electrical potential difference similarly. Thus, in an auto-zero-ized process, it is Node A and Node B and not a true zero current auto-zero electrical potential difference but the approximate value may be generated.

[0048] What should be observed is the point that it is not necessary to generate the true zero current auto-zero electrical potential difference corresponding to the exact zero current which passes along N1 and LED. In this invention, it is desirable to obtain the auto-zero electrical potential difference which can pass a feeble current (about 10nanoampere) through N1 300 and LED 304. Since auto-zero spacing (interval) is about 10microsec, QPC must be about 0.1 picocoulomb extent. As mentioned above, QPC(s) are about 10 picocoulombs.

[0049] Thus, as big effectiveness of QPC, the stabilization auto-zero electrical potential difference of a pixel may easily exceed the sum total of threshold voltage and a turn-on electrical potential difference. Over the whole display, if the auto-zero electrical potential difference with this superfluous condition itself is uniform, it will not become a problem. That is, this effectiveness can be coped with by offsetting all data electrical potential differences suitably.

[0050] However, a problem may be produced when it QPC is not only large, but is influenced by a front data electrical potential difference and the front auto-zero electrical potential difference itself. If this condition occurs within a display, the auto-zero electrical potential difference of all pixels not only becomes superfluous sharply, but the magnitude of excess voltage may differ for every pixel. Under such conditions, a uniform display cannot actually be made by auto-zero-ization of a pixel 300.

[0051] Since this problem is coped with, a pixel 700 can lower Precharge QPC to a very small value. Moreover, the "adjustable precharge" approach that QPC can be changed according to a charge actually required for auto-zero-izing is indicated. When a current auto-zero electrical potential difference is too low, in order to, raise an auto-zero electrical potential difference even to a desired value in short, QPC serves as the minimum value and about 0.1 picocoulombs. However, if a current auto-zero electrical potential difference is too high, QPC will become zero substantially and an auto-zero electrical potential difference will be enabled to fall quickly.

[0052] When drawing 7 is referred to, a pixel 700 consists of five NMOS transistors, N1 (710), N2 (720), N3 (730), N4 (740) and N5 (750), a capacitor 702, and LED (OLED)704 (optical element). Selection Rhine 770 is connected to the gate of a transistor 710. The data line 760 is connected to one terminal of a capacitor 702. The auto-zero line 780 is connected to the gate of a transistor 740. VDD Rhine 790 is connected to the drain of transistors 720 and 750. The auto-zero line 782 from the continued line in a pixel array is connected

to the gate of a transistor 750.
[0053] In this invention, it is the description that the auto-zero line from the continued line can be made into second selection Rhine. That is, it can be made the timing which can use the auto-zero line 782 from the continued line, without needing second selection Rhine for the timing of the present pixel, and the present complexity and the cost of a pixel can be reduced.
[0054] One terminal of a capacitor 702 is connected to the drain of a transistor (setting to Node A) 710. It connects with the gate of transistors (setting to Node B) 720 and 730, and the source of a transistor 710 is connected to the source of a transistor 740. The drain of a transistor 740 is connected to the source of a transistor (setting to Node C) 750, and the drain of a transistor 730. Finally, the source of transistors 730 and 720 is connected to one terminal of LED704.
[0055] Furthermore, a pixel 700 is similar to a pixel 300 concretely except a precharge electrical potential difference being impressed to the node C which is the drain of a transistor N3 (730). Furthermore, there is also some timing modification [like] shown in drawing 8 . Below, actuation of a pixel 700 is divided into the phase of three phases, and is explained.
[0056] The first phase is a precharge phase performed into the front Rhine time (i.e., before data are impressed to the pixel of the continued line). The pulse of plus on selection Rhine turns "ON" N1, by this, Nodes A and B short-circuit mutually and the condition of a pixel 700 returns to the condition after the last auto-zero phase. That is, a pixel returns to the electrical potential difference independent of data which is the latest guess value of the suitable auto-zero electrical potential difference of a pixel. While N1 is "ON", the forward pulse on the auto-zero line 782 from continued-line Rhine turns "ON" a transistor N5, and precharges Node C to Vdd by this. Next, transistors N1 and N5 are set to "OFF."
[0057] Although ON of transistors N1 and N5 and the relative timing of OFF are not so important, a transistor N1 must be set to ON before a transistor N5 is turned off. Otherwise, a transistor N3 may still serve as as [ON] according to the old data electrical potential difference, and the charge poured in to Node C may leak through a transistor N3.
[0058] Charge QPC is saved in Node C after a precharge phase on the capacitance of the gate pair source / drain of transistors N3, N4, and N5. Since the sum total of these capacitance is very small (about 10 fF(s)) and precharge spacing raises Node C by about 10v, QPC(s) are about 0.1 picocoulombs at the beginning. However, this charge is the rate of changing with the approximation precision over the true auto-zero electrical potential difference of a front auto-zero electrical potential difference, and is leaked from Node C before an auto-zero phase. Therefore, for auto-zero-izing, the relation of QPC<=0.1 picocoulomb will be more precisely shown according to how much amount of charges saying whether to be the need. This is the adjustable precharge description. When the last auto-zero electrical potential difference is too low, N3 is un-flowing in a precharge phase, and QPC should stop at the maximum and raises an auto-zero electrical potential difference toward the demand level during an auto-zero phase. When the last auto-zero electrical potential difference is too high, N3 flows, QPC will be leaked by the time an auto-zero phase starts, and the sudden fall of an auto-zero electrical potential difference is attained.
[0059] Although the relative timing of transistors N1 and N5 is not important, desirable timing is shown in drawing 8 . In order to make into the shortest time amount which precharge takes, two transistors N1 and N5 are set to ON at coincidence. Although N1 is off before N5, thereby, leak (it is intentional) of QPC from Node C corresponds to the node B electrical potential difference depressed in capacity by turning OFF N1. Thereby, leak of QPC from Node C certainly corresponds to an equal node B electrical potential difference, when zero data are impressed to a pixel.
[0060] In short, a pixel 700 offers the precharge means of the pixel which enables more effective auto-zero-ization as compared with a pixel 300. Specifically, auto-zero-ization of a pixel 700 is an independence to correctness, quickness, and data more. In the check by computer simulation, a pixel 700 has good auto-zero-izing, and the almost fixed OLED current pair data voltage characteristic can be maintained over the whole term of the actuation life of 10,000 hours.
[0061] Drawing 9 is the schematic drawing of the active-matrix LED pixel structure 900 which are other embodiments of this invention. Although the pixel structure 900 is similar to the pixel structure 700 of drawing 7 , it has additional Vprecharge Rhine 992, and the points which can extend the auto-zero electrical-potential-difference range, without raising the LED supply voltage Vdd differ. This additional correction of a pixel improves the life and effectiveness of a pixel.
[0062] Since Vdd is a precharge electrical potential difference, the pixel (200,300,700) explained above has a limit that an auto-zero electrical potential difference cannot exceed Vdd. However, in order that the threshold voltage of transistors N2 and N3 may carry out a drift over the life period of a transistor and may

amend the drift of TFT drift voltage and an OLED turn-on electrical potential difference, the point which will need to make an auto-zero electrical potential difference higher than Vdd is reached. Since an auto-zero electrical potential difference cannot reach a higher electrical potential difference, the homogeneity of a display deteriorates quickly and marks the end of the useful life longevity of a display. If Vdd is made high, a higher auto-zero electrical potential difference can be attained, but since Vdd is also an OLED drive power source, power effectiveness falls victim.

[0063] Furthermore, if Vdd is lowered and a transistor N2 is operated in the Rhine form field for an improvement of power effectiveness, the range of an auto-zero electrical potential difference will be restricted further. (If it is made such, of course, it is necessary to make N2 larger than the case where it is made to operate by the saturation state) Since an auto-zero electrical potential difference needs to reach level higher than Vdd after short-time actuation in this case, a drive life becomes very short.

[0064] If drawing 9 is referred to, the limit to an auto-zero electrical potential difference is lost to a pixel 700, and modification of the option which makes it possible to fully exceed Vdd by it is included in it. The pixel 900 is the same as a pixel 700, except that train Rhine 992 is added and it is connected to the drain of a transistor 950.

[0065] Train Rhine 992 is added to the array in order to carry the DC electrical potential difference Vprecharge to all pixels. These train [all] Rhine interconnects at the edge of a display. By raising Vprecharge to level higher than Vdd, a pixel 900 can be precharged and auto-zero-ized on an electrical potential difference higher than Vprecharge. ** -- a high value hardly affects display effectiveness.

[0066] Each Vprecharge Rhine 992 should note that the share with the train which a pixel adjoins is possible. This Vprecharge Rhine is run as line Rhine, and the share with an adjoining line is possible for it again.

[0067] In short, in order to extend the range of an auto-zero electrical potential difference exceeding Vdd, the OLED pixel equipped with additional electrical-potential-difference Rhine is indicated. By this, an OLED drive transistor is a required low electrical potential difference on power effectiveness, and it can operate even in the Rhine form field, without restricting an auto-zero electrical potential difference depending on the case. Therefore, a long actuation life and a long well head can be attained. Although this modification was explained about the pixel 700, finally this option modification can carry it out in other auto-zero pixel structures which are not restricted to them including the above-mentioned pixel 200,300.

[0068] although each above-mentioned pixel structure is designed so that the transistor threshold voltage fluctuation and OLED turn-on voltage variation in a pixel may be amended as an object for an OLED display, these pixel structure copes with the heterogeneity generated in the exterior of a pixel -- as -- it is not designed. The usable thing was pointed out to the conventional train drive circuit also after this pixel had united with the display even from the exterior of a display plate.

[0069] Though regrettable, as for an one apparatus data driver, it is common that is not so accurate as an external driver. Although the precision of **12mV can be attained in a commercial external driver, it has become clear in the one apparatus driver that precision of **50mV cannot be attained. An error peculiar to an one apparatus driver type is DC level of a data non-dependency applied to an offset error, i.e., all data electrical potential differences. This offset error changes the value of an ununiformity, i.e., DC level, for every data driver. A liquid crystal display tends to permit an offset error. It is because it is almost exact on the average and a mutual error cannot be recognized by the eye, although a frame drives the reason by sequential antipole nature, an offset error makes liquid crystal dark slightly with a certain frame and it is made bright with the following frame. However, an OLED pixel is driven with single polarity data. Therefore, it does not generate, but if an one apparatus scanner is used, a serious heterogeneity problem may generate bipolar elimination of an offset error.

[0070] Drawing 10 is the schematic drawing of the active-matrix LED pixel structure 300 of this invention connected to the data driver 1010 through the train transistor 1020. This invention explains the elimination approach of the offset error in the one apparatus data scanner for an OLED display. That is, this approach is designed so that it may operate with the pixel of the arbitration which a pixel is connected to a data line in capacity, for example, has an auto-zero phase like the above-mentioned pixels 200,300,500 and 700.

[0071] If drawing 10 is referred to, the above-mentioned pixel 300 is connected to the data line which supplies analog level to a pixel in order to decide the brightness of an OLED element. In drawing 10 , a data line is driven by the data driver which uses the chopped lamp technique (chopped ramp technique) for setting up an electrical potential difference on a data line. The various sources of an error which generate an offset error on a data line exist in this approach (technique). For example, the time amount from which an electrical-potential-difference comparator changes may be changed according to the maximum slew rate

(slew rate) of a comparator. Moreover, changing the maximum slew rate sharply is observed by experiment. An offset error affects the electrical potential difference saved at the pixel. Since the offset error is uneven again, fluctuation of brightness is brought about over the whole display.
[0072] In this invention, the period of auto-zero-izing for a pixel to eliminate the internal threshold error of itself is used also for the calibration of the offset error of a data scanner. The wave of various Rhine is shown in drawing 11 .
[0073] That is, this is attained by setting up criteria black level on a data line using the same train driver as impressing an actual data electrical potential difference. This criteria black level impressed during the auto-zero phase of a pixel is set up on a data line in the completely same way as an actual data electrical potential difference being set up. That is, in the time amount defined by the electrical-potential-difference comparator, the chop of the data lamp (data ramp) is carried out. Therefore, the electrical potential difference which crosses the capacitor C of a pixel becomes settled with the combination which added the offset error electrical potential difference to the turn-on electrical potential difference and black level of a pixel. Criteria black level is maintained during the whole term of an auto-zero phase. If actual data are impressed to a pixel, a data scanner offset error will be eliminated by the electrical potential difference saved on the capacitor of a pixel.
[0074] This technique is applicable not only to the one apparatus scanner which uses a chopped lamp but the scanner which uses a direct sampling to up to a train. When, as for an error, a train (it is big) transistor is turned OFF in a direct sampling, it generates by the ununiformity capacity feed through to the data line of a gate signal. Threshold voltage fluctuation of this transistor produces an ununiformity offset error completely like the ununiformity offset error produced with a chopped lamp data scanner.
[0075] Therefore, this can be amended similarly. Black reference voltage is written in a train during the auto-zero phase of a pixel. Since all a party's pixels auto-zero-ize to coincidence, this black level is written in all data streams at coincidence at the time of the Rhine time initiation. Black level is maintained throughout [whole term / of an auto-zero phase]. Like [in the case of a chopped lamp scanner], if actual data are impressed to a pixel, an offset error will be eliminated by the electrical potential difference saved at the pixel capacitor. However, a time amount overhead required for amendment of an offset error is considered for there to be [which uses direct sampling technique] rather than [little] using chopped lamp technique.
[0076] The approach of this invention for amending a data driver error should enable creation of the homogeneous far good organic LED display of brightness rather than the option. The approach explained here and the auto-zero-ized pixel of one of the above can be used, and the brightness homogeneity of 8 bits without degradation which was conspicuous in homogeneity over all the lives of a display can be attained.
[0077] Although the above-mentioned indication described two or more pixel structures which can be used since the heterogeneity of the brightness of a display is coped with, an external means can amend heterogeneity as substitute approach (technique). More specifically, the following indication explains the approach and the external calibration circuit for coping with the heterogeneity of the brightness of a display. In short, the heterogeneity which measured heterogeneity, saved and was measured can be used about all pixels, and the calibration of data (for example, data electrical potential difference) can be performed.
[0078] Thus, in the following explanation, although the conventional pixel structure of drawing 2 is used, the external calibration circuit and approach of this invention can be used for other pixel structures which are not restricted to these including the above-mentioned pixel 300,500,700. However, if heterogeneity is coped with by the external calibration circuit and approach of this invention, easier pixel structure can be adopted as a display and the yield and the fill factor (fill-factor) of a display can be made to increase by it.
[0079] Drawing 12 is the schematic drawing in the condition of having interconnected and having considered the array (set) of a pixel 200 as the pixel block 1200. If drawing 2 is referred to, in the case of actuation, data will be the approach ordinarily performed with an active matrix display, and will be written in a pixel array. That is, by driving selection Rhine highly, the party of a pixel is chosen and an access transistor N1 serves as ON by it. By impressing a data electrical potential difference to each data line, data are written in each pixel of this line. After the electrical potential difference in Node A is stabilized, this line is canceled of selection by driving selection Rhine low. This data electrical potential difference is saved at Node A until this line is chosen with the following frame. Since there is possibility of some charge leaks from Node A and the voltage drop of unsuitable level is prevented while N1 is turned OFF, an accumulation-of-electricity capacitor may be needed for Node A. The broken line in drawing shows the connection method of a capacitor for coping with a voltage drop. However, such sufficient capacitance may exist in relation to the gate of N2 that the capacitor of such an addition is made unnecessary.

[0080] In what should be observed, the brightness L of OLED was proportional to the current I mostly, and its proportionality constant is considerably stable over the whole display surface. Therefore, if the OLED current decided good is generated, a display will become homogeneity visually.
[0081] However, a pixel is supplied the gate voltage on not an OLED current but N2 by the program. TFT threshold voltage and a mutual conductance (transconductance) may present some initial heterogeneity crossed to the whole display, as the electrical parameter of OLED presents. Furthermore, it is common knowledge that TFT threshold voltage increases under bias temperature stress conditions like an OLED turn-on electrical potential difference. Therefore, these parameters are ununiformities at the beginning, it is a mode depending on each bias hysteresis of each pixel, and it is expected that it changes over all the lives of a pixel. If the program of the gate voltage of N2 is created without amending these parameters, a display will be uneven from the beginning and heterogeneity will increase gradually over all the lives of a display.
[0082] This invention is the approach which the OLED current which the electrical parameter of TFT and OLED was amended and was decided by it good produces in a pixel array. The approach for amending the data electrical potential difference impressed to N2 is explained below.
[0083] Drawing 2 and drawing 12 show the pixel array which has the VDD supply line arranged at juxtaposition at the data line. (In a desirable embodiment, VDD Rhine can wire juxtaposition in selection Rhine.) Thus, a pixel can share each VDD Rhine between two pieces or the adjoining train beyond it, and can reduce the number of VDD Rhine. Drawing 12 shows the condition that VDD Rhine banded together and was blocked around the display. There may be many VDD Rhine included in each pixel block 1200 like the total of VDD Rhine on a display at least as one. However, each pixel block 1200 includes in a desirable embodiment, about 24 VDD Rhine, i.e., the pixel train of about 48.
[0084] Drawing 13 is the schematic drawing of interconnect with a display 1310 and a display controller 1320. A display 1310 consists of two or more pixel blocks 1200. A display controller 1320 consists of the VDD control module 1350, the measurement module 1330 and various I/O devices, for example, an A/D converter, and the memory for saving a pixel parameter.
[0085] Each pixel block is connected to the detection pin (VDD/SENSE) 1210 in the edge of a display, as shown in drawing 12 and 13. During the usual display actuation, the detection pin 1210 is changed to 10 thru/or a 15-volt external Vdd power source, and supplies the current for turning on an OLED element by this to a display. Furthermore, specifically, each VDD/SENSE pin 1210 is connected to the p channel transistors P1 (1352) and P2 (1332) and the current detecting circuit 1334 of a pair in the display controller 1320. During the usual actuation, the ILLUMINATE signal from a display controller operates P1, and connects a VDD/SENSE pin to a Vdd power source. In a typical embodiment, the currents which pass along P1 are expected to be about 1mA / train.
[0086] In order to amend the parameter of TFT and OLED, in order to collect the information about the parameter of each pixel, the external current detecting circuit 1334 is specially operated through a MEASURE signal among a measurement cycle. The collected information is used for the count and adjustment of a data electrical potential difference suitable for realizing a required OLED current during the usual display actuation.
[0087] Furthermore, all other pixels in the measurement cycle of a specific pixel and within a pixel block are turned OFF, and enable it to specifically disregard the drawer of the current from "OFF" pixel certainly by it by impressing a low data electrical potential difference (for example, below zero) to them. Next, the current pulled out by the target pixel is measured according to the impression data electrical potential difference of one or more pieces. A data pattern (that is, it is [certain] under block, and only one pixel is ON, in addition all pixels are off) is impressed to a pixel by the usual approach among each measurement cycle, data are impressed to DATA Rhine by the data driver circuit, and one line is chosen at a time. Thus, since a display is divided by two or more pixel blocks, two or more pixels can be measured by turning ON at least one pixel in each pixel block.
[0088] The current pulled out by the object pixel within each pixel block is measured in P2 from the exterior by driving on the level which connects a detection pin to the input of the current detecting circuit 1334 by P2 course while it separates the VDD/SENSE pin 1210 for ILLUMINATE Rhine and MEASURE Rhine from a VDD power source. Pixel currents are expected to be 1 thru/or 10microA. Although the current detecting circuit 1334 is shown in drawing 13 as mutual impedance amplifier, a current detecting circuit can also be carried out with other gestalten. In this invention, amplifier generates the electrical potential difference proportional to the current in an input edge in an outgoing end. These measured information is collected by I/O device 1340, and this information is changed into a digital format there, and it is saved at the calibrations of a data electrical potential difference. The resistor in the current detecting circuit 1334 is

about 1 megohm.
[0089] Although correspondence of a pixel block and one to one has shown two or more current detecting circuits 1334, if multi-PUREKKUSA (un-illustrating [multi-plexer,]) is used, the number of current detecting circuits can be reduced. That is, two or more VDD/SENSE pins can be multiplexed to the single current detecting circuit 1334. When extreme, a single current detecting circuit can be used for all displays. Although the complexity of an external circuit can be reduced if a VDD/SENSE pin is multiplexed to a detecting circuit in this way, the display measuring time becomes long.
[0090] Since the usual display actuation must be interrupted in order to perform a pixel measurement cycle, pixel measurement must plan timing so that it may not interfere with those who see as much as possible. Since a pixel parameter changes gradually, it is not necessary to measure a specific pixel frequently, and a measurement cycle can be distributed over a long period of time.
[0091] Although it is not necessary to measure all pixels to coincidence, coincidence measurement is advantageous in order to avoid the heterogeneity based on an adjustable measurement lug (delay). This can be attained by measuring all pixels quickly, when a display module turned ["turning on"] on or "is turned off" off. Although it will not become the obstacle of the usual actuation if a pixel is measured when a display module is "OFF", the saved pixel parameter has the fault that homogeneity may not be guaranteed any longer, in long "OFF" period. However, if the power source which is not interrupted is available (setting for example, in screen saver mode), while a display is "OFF" (from a user's viewpoint), a measurement cycle can be performed periodically. Of course, as the option of the arbitration which includes no quick measurement of pixels when a display module is "ON", when power is "OFF", it is required for the nonvolatile memory for saving measurement information to be available.
[0092] If pixel measurement information is available, since the various causes of the heterogeneity of a display will be amended, amendment or the calibration of a data electrical potential difference is applicable to a display. For example, since threshold voltage fluctuation of a transistor and OLED turn-on voltage variation are coped with, a data electrical potential difference can be amended. Therefore, two or more approaches of amending the above and other display heterogeneity are explained below. If these approaches are used, even if some of [some] them have the cause of big heterogeneity in a display, a uniform high-definition display can be offered.
[0093] In order to explain this amendment approach, on a display, it is assumed that it is what uses the pixel structure of drawing 2 . However, this amendment approach is applicable also to the display which used the pixel structure of other arbitration.
[0094] If drawing 2 is referred to, the electrical potential difference saved at Node A will be the gate voltage of N2, therefore the current which passes along N2 and LED will be decided. An LED current can be changed by changing the electrical potential difference on N2. The relation between the gate voltage on N2 and the current which passes along LED is taken into consideration. Gate voltage Vg can be divided into two of the electrical potential differences Vdiode which cross the gate pair source electrical potential differences Vgs and LED of N2 like the following formulas (2).
[0095]
[Equation 2]

$$V_g = V_{gs} + V_{diode} \qquad (2)$$

[0096] The drain current of the MOS transistor of a saturation state is expressed with the following formulas (3).
[0097]
[Equation 3]

$$I = \frac{2}{k}(V_{gs} - V_t)^2 \qquad (3)$$

[0098] Here, k is the mutual-conductance parameter of a device and Vt is threshold voltage (the actuation in the Rhine form field is referring to the following). Therefore, the following formulas (4) are obtained.
[0099]
[Equation 4]

$$V_{gs} = \sqrt{\frac{2I}{k}} + V_t \qquad (4)$$

[0100] The positive current which passes along OLED is expressed with the following formulas (5).
[0101]
[Equation 5]

$$I = AV_{diode}^{m} \qquad (5)$$

[0102] Here, A and m are constants (Burrows other J.Appl.Phys.79 (1996) reference). Therefore, the following formulas (6) are obtained.
[0103]
[Equation 6]

$$V_{diode} = \sqrt[m]{\frac{I}{A}} \qquad (6)$$

[0104] Therefore, the overall relation between gate current and a diode current is expressed with the following formulas (7).
[0105]
[Equation 7]

$$V_g = V_t + \sqrt{\frac{2I}{k}} + \sqrt[m]{\frac{I}{A}} \qquad (7)$$

[0106] Although other functional forms can also be used since the I-V property of OLED is expressed, according to the above-mentioned formula, it should note bringing about the functional relation from which it differs between gate current and a diode current. However, this invention can be fitted so that it may not be limited to a function form with the detailed I-V property of above OLED, therefore may operate about the diode-property of arbitration.
[0107] The brightness L of OLED is proportional to the current I mostly, and a proportionality constant's is stable and uniform over the whole display surface. If the OLED current decided good can be generated, a display will serve as homogeneity visually. However, as explained above, the pixel is programmed not using the current I but using the electrical potential difference Vg. The problem is the point that the parameters Vt and k of TFT other than the parameters A and m of OLED cross all over a display, and present a certain amount of initial heterogeneity. Furthermore, it is common knowledge that Vt increases under bias temperature stress conditions. It is known that the OLED parameter A will decrease under bias stress directly in relation to the turn-on electrical potential difference of OLED. The OLED parameter m has relation in distribution of the trap in an organic band gap, and changes over all the lives of OLED. Therefore, it is expected that these parameters are uneven in early stages, and it changes over all the lives of a display depending on each bias hysteresis of each pixel. If gate voltage is programmed without amending fluctuation of these parameters, a display will be uneven in early stages and heterogeneity will increase over all the lives.
[0108] There is actually another cause of heterogeneity. Gate voltage Vg is not necessarily equal to the meant data electrical potential difference Vdata. The gain error in a data driver, an offset error, and the feed through (data dependency) generated from selection discharge of N1 make these two electrical potential differences produce a difference rather. These causes of an error are also uneven, and it changes over all the lives of a display. The above, and other gain errors and offset errors are expressed with the following formulas (8).
[0109]
[Equation 8]

$$V_g = BV_{data} + V_0 \qquad (8)$$

[0110] Here, B and V0 are a gain factor and offset voltage, respectively, both, are uneven and are obtained. If it arranges combining a formula (7) and (8), the following formulas (9) will be obtained.
[0111]
[Equation 9]

$$V_{data} = V_{off} + C\sqrt{I} + D\sqrt[m]{I} \qquad (9)$$

[0112] Here, Voff, and C and D are the above-mentioned parameter combination.
[0113] Since this invention amends fluctuation of Voff, and C, D and m, it offers the various amendment approaches which amend the data (input) electrical potential difference to mean, and enables generating of the OLED current in a pixel array decided good by it. Since fluctuation of Parameter Voff, and C, D and m is amended, the above-mentioned external current detecting circuit can measure from the outside the current pulled out by the information about each pixel, i.e., a single pixel. The information measured about Parameter Voff, and C, D and m is used, and during the usual display actuation, this invention calculates the suitable data electrical potential difference Vdata according to a formula (9) in order to decide a required OLED current.
[0114] Moreover, it becomes expensive by computer to calculate correctly four parameters Voff, and C, D and m from the measured value of a current, and complicated repeat count is needed. However, the good approximation which reduces the complexity of count can be used, maintaining effective amendment.
[0115] In a desirable embodiment, the ununiformity property of a pixel can be expressed as mentioned above using only two parameters instead of four pieces. When the current potential property of the pixel of a formula (9) is referred to, in the usual lighting level, the CrootI term about Vgs of N2 and the DmrootI term about Vdiode are the almost same magnitude. However, the dependencies to those pixel currents differ greatly. Since the value of m is about 10, in ordinary lighting level, DmrootI is the function of far weak I as compared with CrootI. For example, if I is made to increase by 100 times, CrootI will increase 10 times, but DmrootI will not increase 1.58 times (if m is assumed to be 10). That is, in ordinary lighting current level, the I-V curve of OLED serves as a steep slope from the I-Vgs curve of TFT far.
[0116] Therefore, in ordinary current level, DmrootI is independent to a current and approximation [fluctuation / for every pixel of the] that it can only process as one offset error is performed. Although this approximation carries in some errors, the appearance of the whole display does not deteriorate sharply. Therefore, the heterogeneity of all displays can be processed as fluctuation of offset and gain in a remarkable precision. Therefore, (9) types can be approximated like the following formulas (10).
[0117]
[Equation 10]

$$V_{data} = V_{offset} + C\sqrt{I} \qquad (10)$$

[0118] Here, it is Voffset. = Voff + DmrootI changes Voffset and C for every pixel including DmrootI.
[0119] Drawing 14 is the flow chart of the approach 1400 of initializing a display by measurement of the parameter of all pixels. An approach 1400 begins from step 1405, and progresses to step 1410, and an "off-" data electrical potential difference is impressed to all pixels other than the pixel made into the object within a pixel block there.
[0120] In step 1420, in order to calculate target specific Voffset and specific C of a pixel, an approach 1400 impresses two data electrical potential differences (V1 and V2), and measures a current about each data electrical potential difference.
[0121] In step 1430, the square root of currents I1 and I2 is calculated. In a desirable embodiment, a square root table is used for this count.
[0122] Voffset and C are calculated in step 1440. That is, two formulas can be used for asking for two variables. Next, Voffset and C which were asked for the specific object pixel are saved at storage, for example, memory. If measurement of all pixels finishes, memory saves two parameters Voffset and C about each pixel in an array. These values are behind applicable to the calibration of Vdata, or adjustment using a formula (10). An approach 1400 is ended in step 1455 next.
[0123] The current which passes along the pixel measured should note fully having to be high so that DmrootI may become almost equal in two point of measurement. As for this condition, it is desirable that it may be made satisfied by performing one measurement in the highest data electrical potential difference which a system can generate, and then performing measurement of another side in a slightly low data electrical potential difference.
[0124] If initialization of a display is performed, the raw input video data supplied to the display module is correctable. The input video data should note being able to exist in various formats, such as for example, (1) pixel electrical potential difference, pixel brightness by which (2) gamma corrections were carried out, or (3) pixel current. Therefore, it depends on each specific format for use of the parameters Voffset and C with

which it was saved for performing the calibration of an input video data, or amendment.
[0125] Drawing 15 is the flow chart of the correction approach 1500 of the input video data showing a pixel electrical potential difference. An approach 1500 begins from step 1505, and progresses to step 1510, and the parameter saved about the object pixel there, for example, Voffset and C, is taken out.
[0126] In step 1520, an approach 1500 impresses the taken-out parameter in order to perform the calibration of an input video data. Bias has not started an input video data, i.e., more specifically, it is expected that a zero bolt expresses zero brightness and larger data than zero express a larger intensity level than zero. Therefore, it can be considered that an electrical potential difference is equal to C0 rootI. Here, I is [the constant of a need current and C0, for example, a typical value,] 103V/rootA. In order to amend the pixel fluctuation at the time of an input video data going into a display module, it is Voffset about each pixel. = Voff + CrootI is calculated based on Voffset and C which were saved. This count consists of hanging C/C0 on a video data, and adding Voffset to that result. The division by C0 is unnecessary if the video data Vdata is already reduced by fixed multiplier 1 / C0 fixed. Multiplication by C can be performed by digital logic using direct or a look-up table. For example, in the case of the latter, each value of C specifies the table whose table entry is as a result of multiplication while the value of a video data is an index. (Or the input video data in a look-up table and the role of C can also be made reverse.) After multiplication is performed, rapid addition of Voffset is performed by digital logic.
[0127] In step 1530, the obtained electrical potential difference Vdata, i.e., the input data corrected or adjusted, is sent to the data driver of a pixel array. An approach 1500 is ended at step 1535 next.
[0128] In the case of the brightness data by which the gamma correction was carried out, an input video data is proportional to L0.45. Here, L is brightness. This is typical in the video data beforehand amended about the CRT brightness-voltage characteristic. It is L0.45=rootL, and since OLED brightness is proportional to the current, data can be processed as a thing proportional to rootI. Therefore, count can be performed by the approach about the zero offset electrical potential difference explained previously, and the same approach.
[0129] Drawing 16 is the flow chart of the amendment approach 1600 of the input video data showing a pixel current, i.e., brightness. An approach 1600 begins from step 1605, and progresses to step 1610, and the value of the square root of the current measured there is calculated. That is, the approach 1600 is the same as the above-mentioned approach 1500 except being processed so that the video data showing I may generate rootI. As mentioned above, this operation can be performed from a pixel amperometry value using the table which gives the value of a square root required to ask for the pixel parameters Voffset and C, as shown in drawing 14 . rootI is again generated from a video data here using this table.
[0130] Next, the data correction step 1610 thru/or 1645 are the same as that of the above-mentioned approach 1500 except asking for the data electrical potential difference which hung C on the input data in step 1630, then added Voffset, and was amended.
[0131] Or in another embodiment, the ununiformity property of a pixel can be expressed as mentioned above not using two pieces or four parameters but using one parameter. That is, as the ununiformity property of a pixel is expressed using a single parameter, it is simplified further.
[0132] Furthermore, in many cases, fluctuation of gain factor C for every pixel is small, and, specifically, only Voffset remains as a significant cause of heterogeneity. This is generated when the TFT mutual-conductance parameter k and electrical-potential-difference gain factor B are homogeneity. In this case, it is enough if only Voffset of each pixel is calculated. If it does so, data correction will not perform multiplication (since it is considered that a gain factor is uniform), but will perform only addition of an offset parameter.
[0133] This single parameter technique is similar to the above-mentioned auto-zero-ized OLED pixel structure. This single parameter amendment approach should produce the display homogeneity which should be satisfied while reducing computer costs. However, in use of a specific display with very important homogeneous maintenance of a display, even if the complexity and costs of a computer increase, two above-mentioned pieces or the above-mentioned four-piece parameter approach can be used.
[0134] Here, a display initialization process is influenced by format (format) of data about single electrical parameter extraction and data correction. The single parameter technique is applicable to initialization of a display, and amendment of a video data, when a video data expresses (1) pixel electrical potential difference, (2) pixel current, and the pixel brightness by which (3) gamma corrections were carried out.
[0135] Drawing 17 shows the flow chart of the initialization approach of the display by measurement of the parameter of all pixels. An approach 1700 begins from step 1705, and progresses to step 1710, and an "off-" data electrical potential difference is impressed to all pixels other than the object pixel within a pixel block there. In step 1720, in order to calculate target specific Voffset and specific C about a pixel, an approach

1700 impresses the data electrical potential difference (V1 and V2) of two pieces, and measures a current for every data electrical potential difference.
[0136] In step 1730, the square root of currents I1 and I2 is calculated. In a desirable embodiment, a square root table is used for this count.
[0137] Since it is thought that the value of C is uniform, it should note being able to ask for it by performing two-point measurement in the location of the arbitration in a display ideally. However, since this may have the unusual object pixel, it may have a problem. Therefore, two-point measurement is performed for every pixel.
[0138] The average of C is calculated in step 1740. Namely, the average of C of a display can be calculated by using the table for calculating rootI about each amperometry value.
[0139] In step 1750, the average C is used from the amperometry value of each pixel, and Voffset of each pixel is calculated. Thus, small fluctuation of C covering the whole display is partially amended by count of Voffset. It is desirable to measure measurement of the current of each pixel in the possible highest data electrical potential difference for the reason for the above.
[0140] Finally in step 1760, Voffset of each pixel is saved at storage, for example, memory. Next, an approach 1700 is ended in step 1765.
[0141] Drawing 18 is the flow chart of the amendment approach 1800 of the input video data showing a pixel electrical potential difference. An approach 1800 begins from step 1805, progresses to step 1810, and takes out the parameter Voffset saved about the object pixel there.
[0142] In step 1820, an approach 1800 performs the calibration of an input video data using the taken-out parameter Voffset. More specifically based on the value of saved Voffset, it is Vdata about each pixel. = Voffset+Vdata A value is calculated.
[0143] In step 1830, the obtained input data which was Vdata(ed), namely, amended or adjusted is sent to the data driver of a pixel array. Next, an approach 1800 is ended in step 1835.
[0144] Drawing 19 is the flow chart of the initialization approach 1900 of the display by measurement of the parameter of all the pixels about the situation that a video data expresses a pixel current. There is a close resemblance between an approach 1900 and the above-mentioned approach 1700. The difference with the above-mentioned approach 1700 is the case where use the average value of C by which it was calculated by the approach 1900 having taken in additional step 1950, and the table of a zero offset data electrical-potential-difference pair pixel current is created. A square root operation is not performed by using this table in previous initialization and a previous data correction process from this point. This table is a precision higher than a square root function, and it is expected that the current-voltage characteristic of a pixel is expressed. Next, since this table uses it later, it is saved by it at storage, for example, memory. Next, each pixel amperometry value is used as an index for putting into this table, and each pixel offset Voffset is searched for.
[0145] Drawing 20 is the flow chart of the amendment approach 2000 of the input video data showing a pixel current, i.e., brightness. An approach 2000 begins from step 2005, progresses to step 2010, and takes out Voffset of the pixel made into a current object there from storage.
[0146] In step 2020, it asks for a zero offset data electrical potential difference from an input video-data current using the table of a zero offset data electrical-potential-difference pair pixel current. In step 2030, this zero offset data electrical potential difference is applied to taken-out Voffset. Finally, in step 2040, the input video data amended or adjusted is sent to the data driver of a pixel array.
[0147] In short, if a video data is introduced into a display module, the zero offset data electrical potential difference corresponding to each current will be searched in a V-I table. Next, the pixel offset saved is added to zero offset voltage, and the result serves as an input to a data driver. An approach 2000 is ended in step 2045 next.
[0148] Drawing 21 is the flow chart of the initialization approach 2100 of the display by measurement of the parameter of all the pixels about the situation of expressing the brightness data with which the gamma correction of the video data was carried out. There is a close resemblance between an approach 2100 and the above-mentioned approach 1900. The difference with an approach 2100 and the above-mentioned approach 1900 is a time of creating the table of the square root of a zero offset data electrical-potential-difference pair pixel current using the average value of calculated C in step 2150. That is, a video data can be made to approximate as a thing showing rootI. Therefore, the zero-offset table of Vdata pair rootI is created using the average of C, and this table is saved at storage, such as memory.
[0149] Drawing 22 is the flow chart of the amendment approach 2200 of the input video data showing the brightness data by which the gamma correction was carried out. There is a close resemblance between an

approach 2200 and the above-mentioned approach 2000. The difference with the above-mentioned approach 2000 is generated in the zero-offset table of Vdata pair rootI. Therefore, in short, a zero offset data electrical potential difference is looked for using the video data which enters, and the saved pixel offset is added to these electrical potential differences.

[0150] In the above-mentioned explanation, it is regarded as that to which the OLED drive transistor N2 operates by the saturation state. If N2 operates in the Rhine form field, the similar amendment approach can be used. In that case, the current potential property of a pixel is expressed with the following formulas (11).

[0151]

[Equation 11]

$$V_{data} = V_{off} + C(I)I + D\sqrt[m]{I} \qquad (11)$$

[0152] Here, C (I) is the weak function of I. Here, as mentioned above, if a current is fully high to extent which should ask only for an offset term and a gain factor, a DmrootI term can be included in it at a Voff term. However, since gain factor C (I) contains the uneven OLED parameters A and m, the single parameter approximation which considers that only offset voltage is an ununiformity is not expected to be as accurate as the single parameter approximation about the case of the above-mentioned saturation. Therefore, if N2 operates in the Rhine form field, the two-piece parameter amendment approach will be considered to be far powerful rather than the single parameter amendment approach.

[0153] Drawing 23 is the block diagram of the system 2300 which used the display 2320 equipped with two or more active-matrix LED pixel structures 300, 500, or 700 of this invention. A system 2300 consists of a display controller 2310 and a display 2320.

[0154] Furthermore, specifically, a display controller can be taken as a central processing unit CPU (2312), memory 2314, and the general purpose computer that has two or more I/O devices (for example, various modules, such as stores, such as a mouse, a keyboard, a magnetic device, and optical equipment, a modem, an A/D converter, and the above-mentioned measurement module 1330). The software instruction (for example, the above-mentioned various approaches) for operating a display 2320 can be loaded to memory 2314 from a storage, and can be executed by CPU2312. Therefore, the software instruction of this invention can be saved to the medium which can be read by computer.

[0155] A display 2320 consists of the pixel interface 2322 and two or more pixels (pixel structures 300, 500, or 700). The pixel interface 2322 includes a circuit required for the drive of pixels 300, 500, or 700. For example, the pixel interface 2322 can be considered as a matrix addressing interface as shown in drawing 1 , and can include the additional above-mentioned signal line/control line as an option.

[0156] Therefore, a system 2300 can be carried out as a laptop computer. Or a display controller 2310 can carry out as a microcontroller or the integrated circuit (ASIC) of a specified use, or combination of hardware and a software instruction. In short, a system 2300 can be carried out in the big system incorporating this invention.

[0157] Although this invention was explained as what uses an NMOS transistor, this invention is realizable even if it uses the PMOS transistor which the related electrical potential difference reversed.

[0158] As mentioned above, although the various embodiments of this invention were shown in this specification and explained to the detail, many modes can be taken unless the summary of this invention is exceeded.

[0159]

[Effect of the Invention] The homogeneity of brightness is improved sharply and, as for the display of this invention, the industrial value is high.

[Translation done.]

* NOTICES *

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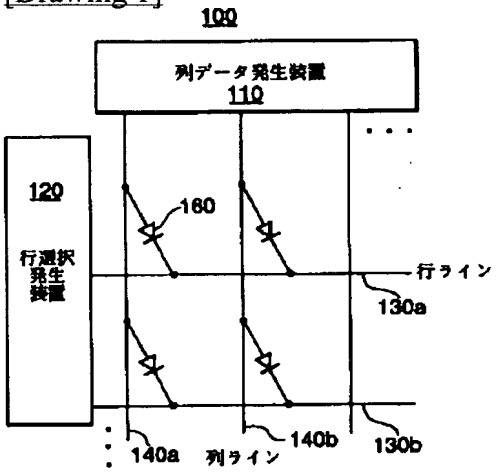
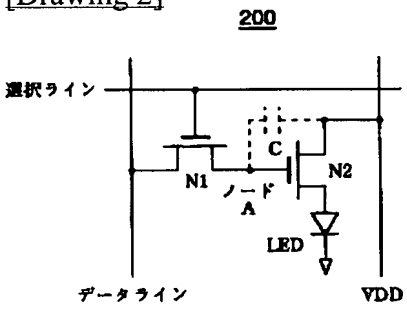
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

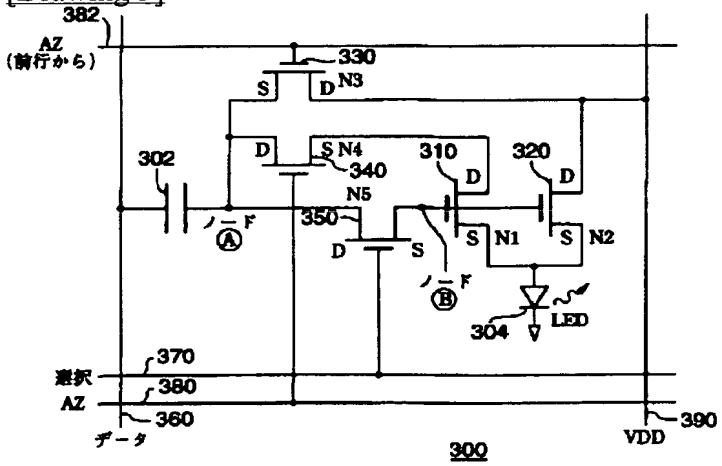
[Drawing 1]



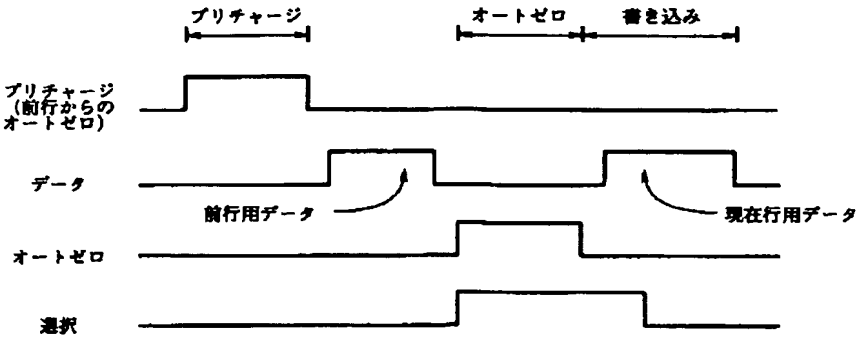
[Drawing 2]



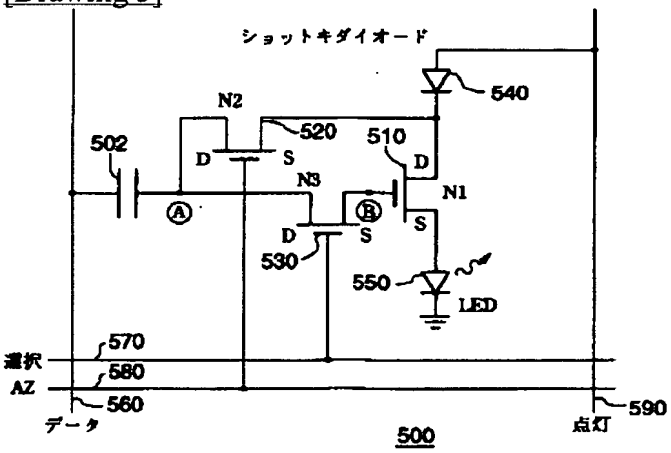
[Drawing 3]



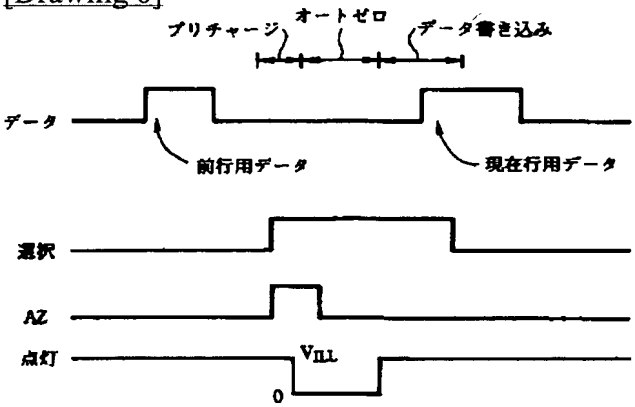
[Drawing 4]



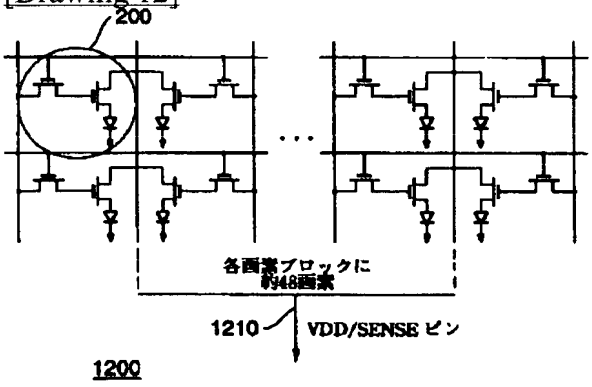
[Drawing 5]



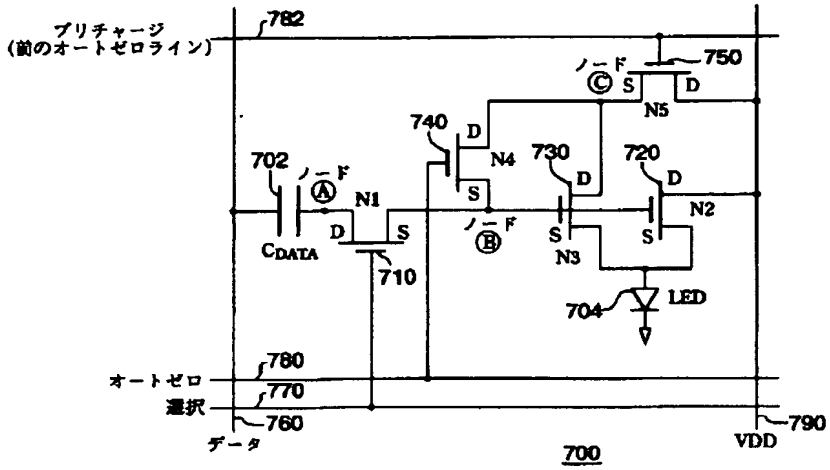
[Drawing 6]



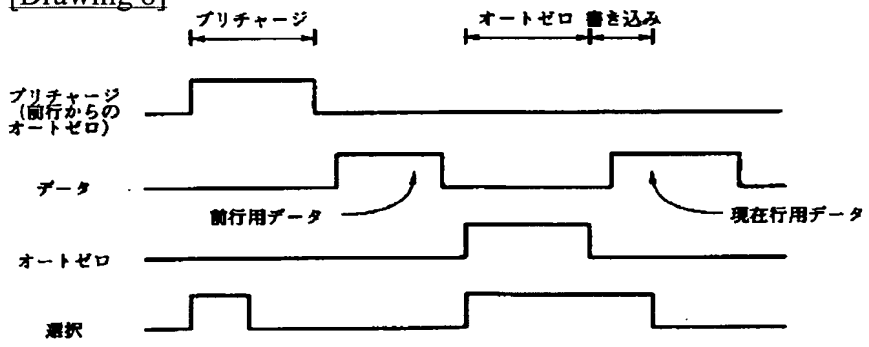
[Drawing 12]



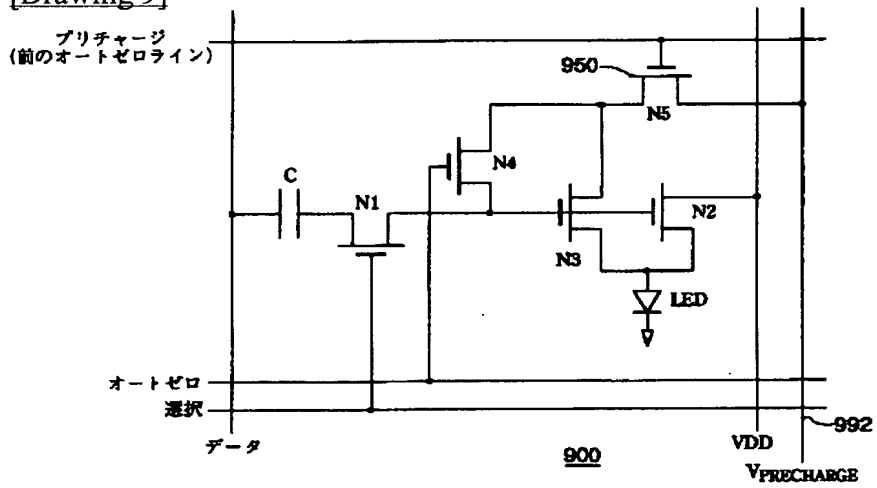
[Drawing 7]



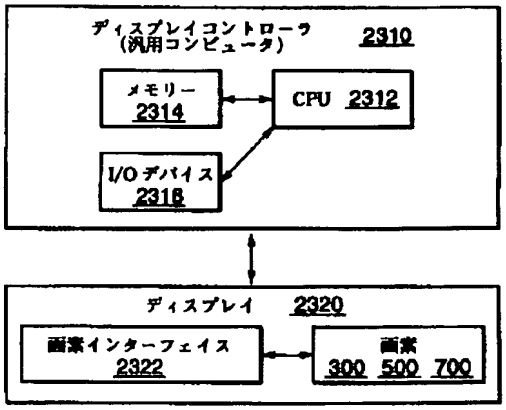
[Drawing 8]



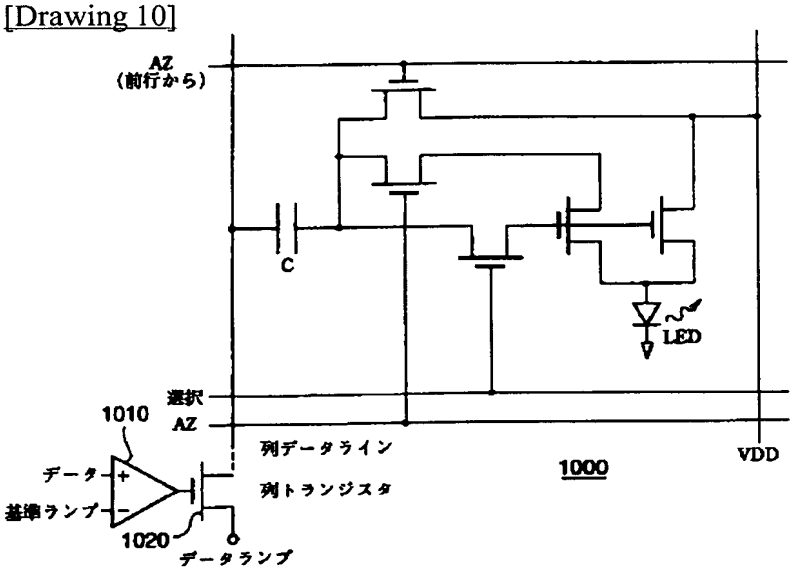
[Drawing 9]



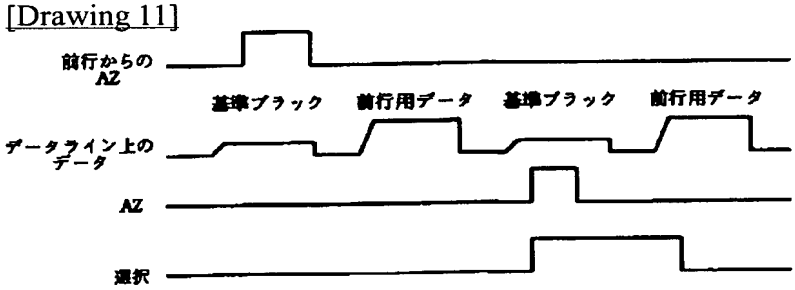
[Drawing 23]



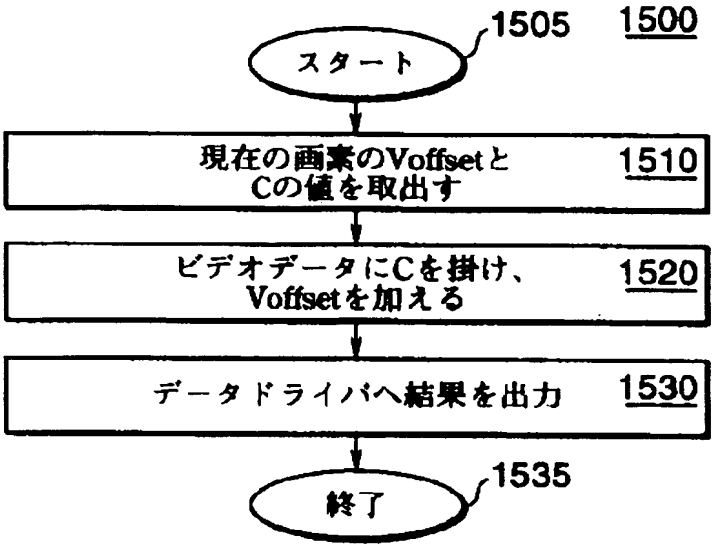
[Drawing 10]



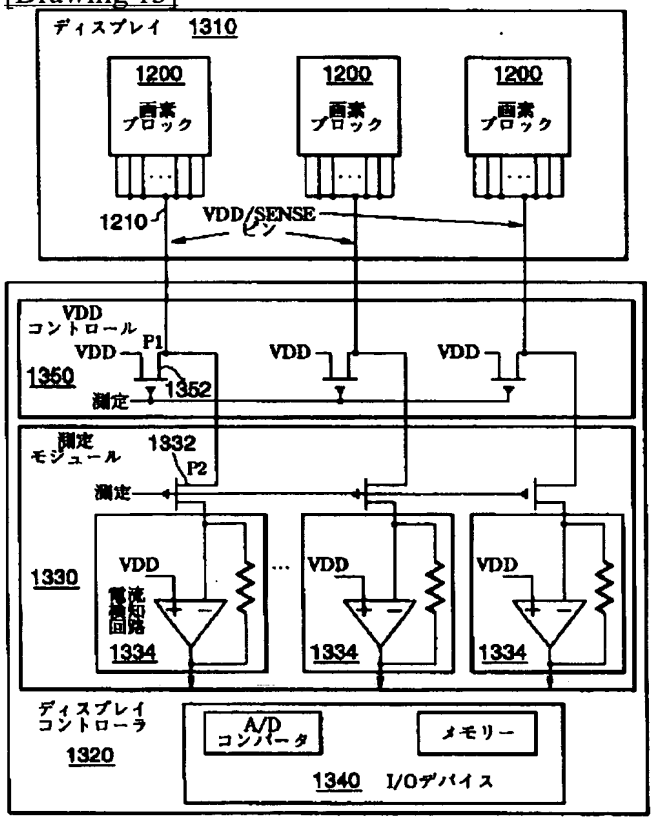
[Drawing 11]



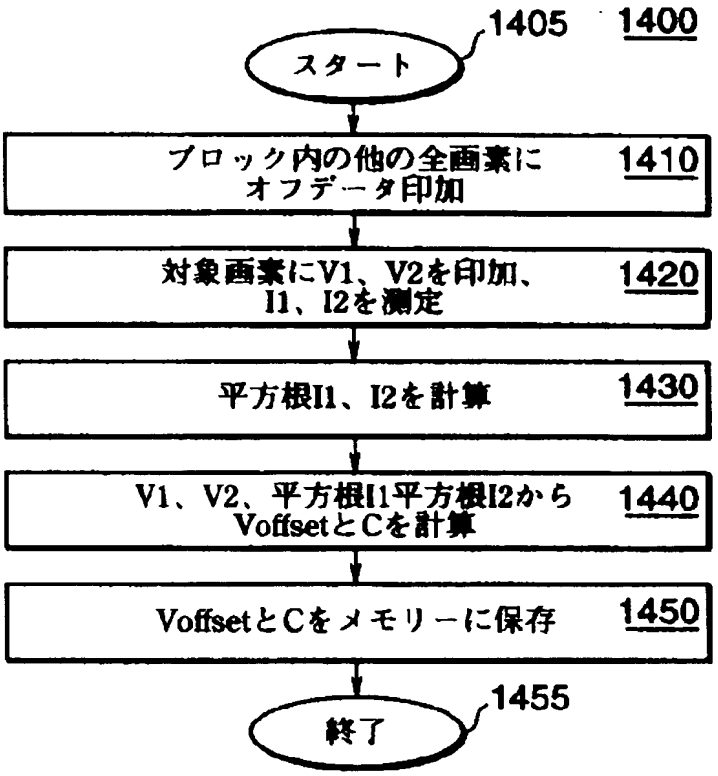
[Drawing 15]



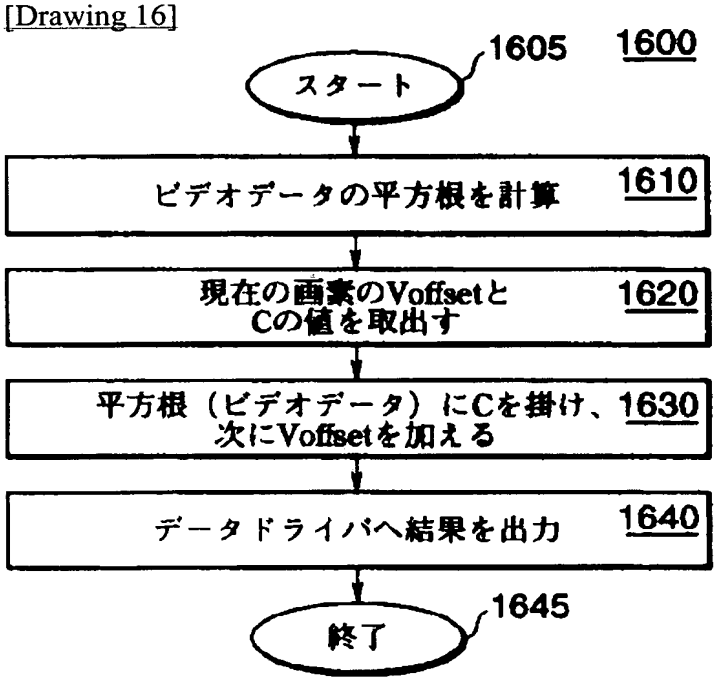
[Drawing 13]



[Drawing 14]

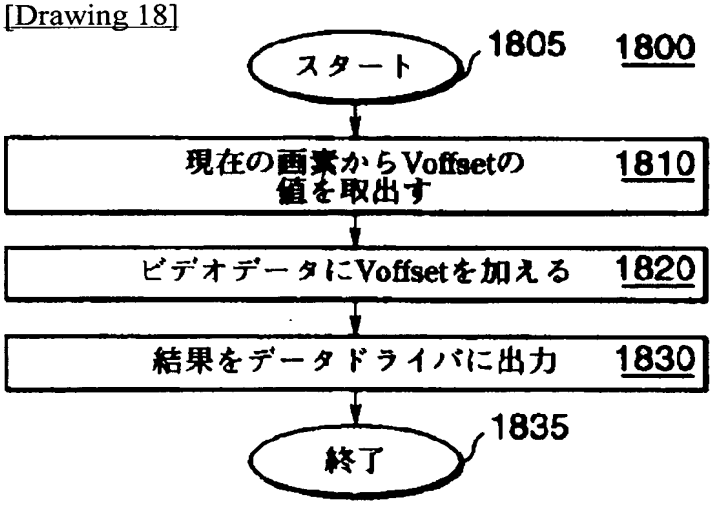


[Drawing 16]



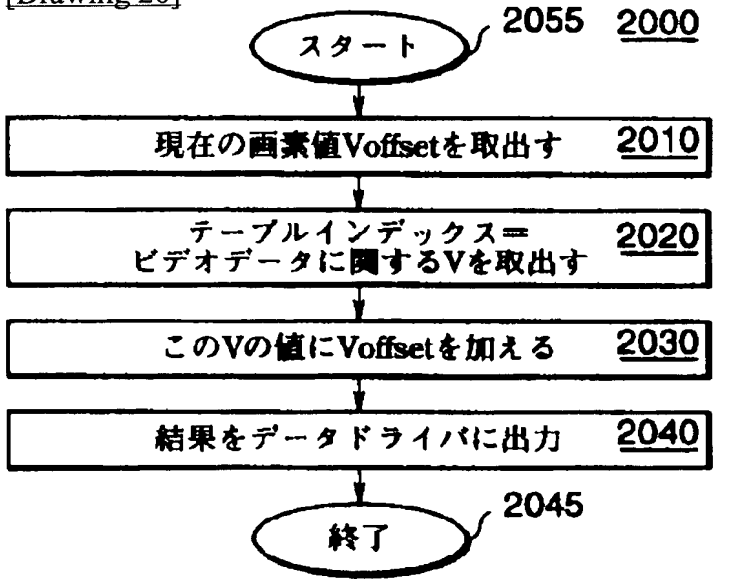
[Drawing 17]

[Drawing 18]



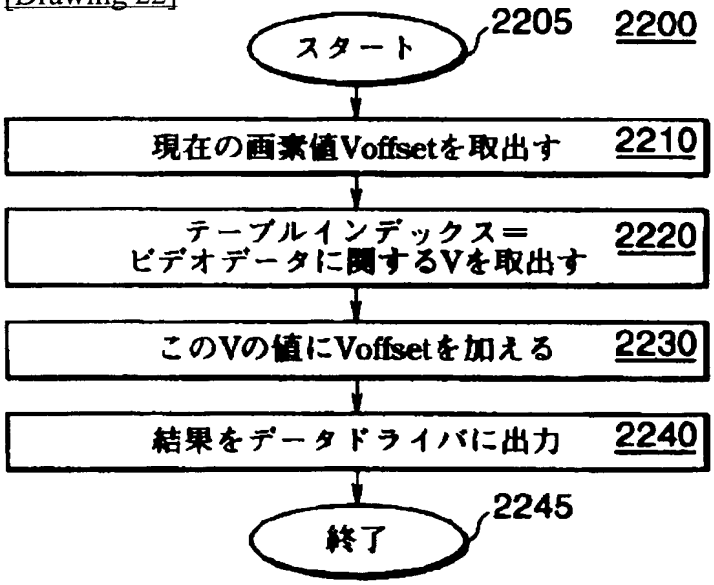
[Drawing 19]

[Drawing 20]



[Drawing 21]

[Drawing 22]



[Translation done.]

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	9/33			9/33	Ｚ
					Ｍ
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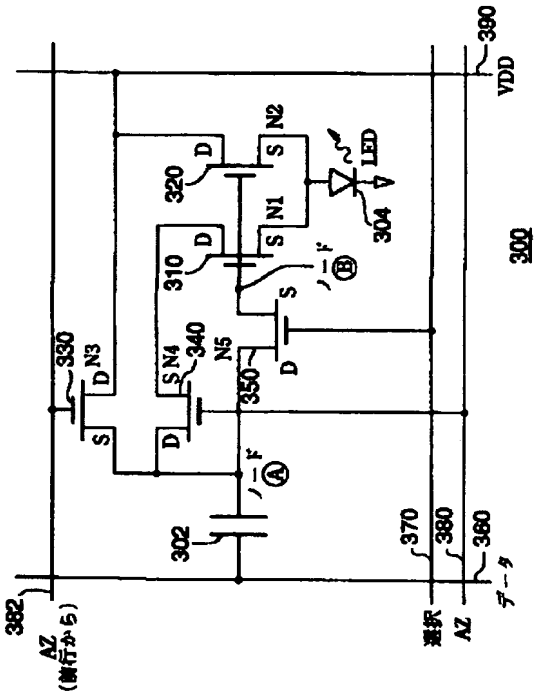
最終頁に続く

(54)【発明の名称】　アクティブマトリックス発光ダイオード画素構造およびその方法

(57)【要約】

【課題】画素構造の発光ダイオードにおける電流の不均一性を低減することによって、輝度の不均一性を改善するＬＥＤ画素構造と方法とを提供する。

【解決手段】少なくとも一つの画素を備えるディスプレイであって、上記画素は、第１トランジスタと、キャパシタと、第２トランジスタと、第３トランジスタと、第４トランジスタと、第５トランジスタと、光要素とから成り、それらの構成要素を特定に接続することにより構成されていることを特徴とするディスプレイ。



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【特許請求の範囲】

【請求項１】　少なくとも一つの画素を備えるディスプレイであって、当該画素は、（１）第１選択ラインへの接続用であるゲートと、ソースと、ドレインとを有する第１トランジスタと、（２）当該第１トランジスタのドレインが接続されている第１端子と、第２端子とを有するキャパシタと（３）オートゼロラインへの接続用であるゲートと、ソースと、当該第１トランジスタの当該ドレインが接続されているドレインとを有する第２トランジスタと、（４）第２選択ラインへの接続用であるゲートと、当該第２トランジスタのドレインに接続されたソースと、ドレインとを有する第３トランジスタと、（５）当該第１トランジスタのソースに接続されたゲートと、ソースと、当該第２トランジスタの当該ソースに接続されたドレインとを有する第４トランジスタと、（６）当該第１トランジスタのソースに接続されたゲートと、ソースと、当該第３トランジスタの当該ドレインに接続されたドレインとを有する第５トランジスタと、（７）当該第４トランジスタのソースと当該第５トランジスタのソースとが、一方の端子に接続されている２個の端子を有する光要素とから成ることを特徴とするディスプレイ。

【請求項２】　前記光要素が有機発光ダイオード（ＯＬＥＤ）である請求項１に記載のディスプレイ。

【請求項３】　前記各トランジスタが非晶質シリコンから造られた薄膜トランジスタである請求項１又は２に記載のディスプレイ。

【請求項４】　前記第２選択ラインが前行からのオートゼロラインである請求項１～３の何れかに記載のディスプレイ。

【請求項５】　少なくとも一つの画素を備えたディスプレイであって、当該画素は、（１）一つの選択ラインへの接続用であるゲートと、ソースと、ドレインとを有する第１トランジスタと、（２）当該第１トランジスタのドレインが接続されている第１端子と、第２端子とを有するキャパシタと、（３）オートゼロラインへの接続用であるゲートと、ソースと、当該第１トランジスタの当該ドレインが接続されているドレインとを有する第２トランジスタと、（４）当該第２トランジスタのソースに接続された第１端子と、点灯ラインへの接続用の第２端子とを有するダイオードと、（５）第１トランジスタのソースに接続されたゲートと、ソースと、当該ダイオードの第１端子に接続されたドレインとを有する第３トランジスタと、（６）当該第３トランジスタのソースが、一方の端子に接続されている２個の端子を有する光要素とから成ることを特徴とするディスプレイ。

【請求項６】　前記ダイオードがショットキダイオードである請求項５に記載のディスプレイ。

【請求項７】　少なくとも一つの画素を備えたディスプレイであって、当該画素は、（１）第１選択ラインへの

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接続用であるゲートと、ソースと、ドレインとを有する第１トランジスタと、（２）当該第１トランジスタのドレインが接続されている第１端子と、第２端子とを有するキャパシタと、（３）オートゼロラインへの接続用であるゲートと、当該第１トランジスタの当該ソースが接続されているソースと、ドレインとを有する第２トランジスタと、（４）第２選択ラインへの接続用であるゲートと、当該第２トランジスタのドレインに接続されたソースと、ドレインとを有する第３トランジスタと、（５）当該第１トランジスタのソースに接続されたゲートと、ソースと、当該第３トランジスタの上記ソースに接続されたドレインとを有する第４トランジスタと、（６）当該第１トランジスタのソースに接続されたゲートと、ソースと、当該第３トランジスタの当該ドレインに接続されたドレインとを有する第５トランジスタと、（７）当該第４トランジスタのソースと当該第５トランジスタのソースとが、一方の端子に接続されている２個の端子を有する光要素とから成ることを特徴とするディスプレイ。

【請求項８】　前記光要素が有機発光ダイオード（ＯＬＥＤ）である請求項７に記載のディスプレイ。

【請求項９】　前記第２選択ラインが前行からのオートゼロラインである請求項７又は８に記載のディスプレイ。

【請求項１０】　（１）少なくとも一つのオートゼロ化画素構造と、（２）当該オートゼロ化画素構造にオートゼロ化の実行を可能にするため、当該オートゼロ化画素構造に接続されたオートゼロラインと、（３）オートゼロ電圧の範囲を拡張するため、一つの電圧を当該オートゼロ化画素構造に運ぶように、当該オートゼロ化画素構造に接続された第２ラインとから成るディスプレイ。

【請求項１１】　光要素への印加エネルギーを制御する回路を含む少なくとも１個の画素を有するディスプレイを点灯する方法であって、（ａ）画素をオートゼロ化するステップと、（ｂ）データライン経由でデータを当該画素へロードするステップと、（ｃ）保存されたデータに基づいて当該光要素を点灯するステップとから成ることを特徴とする方法。

【請求項１２】　前記オートゼロ化ステップ（ａ）の前に前記画素をプリチャージするステップを更に含む請求項１１に記載の方法。

【請求項１３】　前記オートゼロ化ステップ（ａ）が基準ブラックレベルを印加するステップを含む請求項１１又は１２に記載の方法。

【請求項１４】　少なくとも１個の画素を有するディスプレイを点灯する方法であって、（ａ）当該画素の画素パラメータを測定するステップと、（ｂ）測定された画素パラメータに基づいて入力画素データを調整するステップと、（ｃ）調整された入力画素データに基づいて当該画素を点灯するステップとから成ることを特徴とする

方法。

【請求項１５】　前記測定ステップ（ａ）が前記画素によって引き出された電流を外部的に測定する請求項１４に記載の方法。

【請求項１６】　前記調整ステップ（ｂ）が、電圧オフセット（V_{offset}）パラメータを求めるため、前記測定された画素パラメータを使用して前記画素データを補正する請求項１４又は１５に記載の方法。

【請求項１７】　前記調整ステップ（ｂ）が、更に、ゲイン係数（Ｃ）パラメータを求めるため、前記測定された画素パラメータを使用して前記画素データを補正する請求項１６に記載の方法。

【請求項１８】　ディスプレイコントローラと当該ディスプレイコントローラに接続されると供に複数の画素から成るディスプレイとから成るシステムであって、当該各画素が、（１）第１選択ラインへの接続用ゲートと、ソースと、およびドレインとから成る第１トランジスタと、（２）当該第１トランジスタの当該ドレインに接続された第１端子と、第２端子とを有するキャパシタと、（３）オートゼロラインへの接続用ゲートと、当該第１トランジスタの当該ソースに接続されたソースと、ドレインとを有する第２トランジスタと、（４）第２選択ラインへの接続用ゲートと、当該第２トランジスタの当該ドレインに接続されたソースと、ドレインとを有する第３トランジスタと、（５）当該第１トランジスタの当該ソースに接続されたゲートと、ソースと、当該第３トランジスタの当該ソースに接続されたドレインとを有する第４トランジスタと、（６）当該第１トランジスタの当該ソースに接続されたゲートと、ソースと、当該第３トランジスタの当該ドレインに接続されたドレインとを有する第５トランジスタと、（７）当該第４トランジスタのソースと当該第５トランジスタのソースとが、一方の端子に接続されている２個の端子を有する光要素とから成ることを特徴とするシステム。

【請求項１９】　（１）画素の画素パラメータを測定するための測定モジュールと、（２）当該測定された画素パラメータを保存するための記憶装置とを有するディスプレイコントローラと、（３）当該保存された画素パラメータに基づいて調整された入力画素データを表示するため、当該ディスプレイコントローラに接続されたディスプレイとから成るシステム。

【請求項２０】　前記測定モジュールが前記画素によって引き出される電流を測定するための電流検知回路を有する請求項１９に記載のシステム。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、アクティブマトリックス発光ダイオード画素（ピクセル）構造に関する。本発明は、詳しくは、画素構造の発光ダイオードにおいて電流の不均一性を低減して輝度の均一性を改善する画素構造と、前記アクティブマトリックス発光ダイオード画素構造の作動方法に関する。尚、本出願は1997年9月29日出願の米国仮出願第 60/060,386 号および1997年9月29日出願の米国仮出願第 60/060,387 号の優先権を主張すると供に、本出願に引用する。

【０００２】

【従来の技術】図１に示すようなマトリックスアドレッシングを使用して画素を点灯するマトリックスディスプレイは、当該技術分野において周知である。典型的なディスプレイ１００は、行と列に構成された画面要素すなわち表示要素（ピクセル）１６０を有する。このディスプレイは、列データ発生装置１１０と行データ発生装置１２０を内蔵している。作動にあたっては、各行は行ライン１３０を介して順次通電されるとともに、対応する列ラインを使用して対応する画素が通電される。パッシブマトリックスディスプレイにおいては、各行の画素は順次１個ずつ点灯されるが、アクティブマトリックスディスプレイにおいては、各列の画素に順次データがロードされる。すなわち、パッシブマトリックスディスプレイの各列は全フレーム時間のほんの一部分で「通電状態である」に過ぎないが、アクティブマトリックスディスプレイの各列はフレーム時間の全体にわたって「通電状態とする」ことが出来る。

【０００３】ポータブルディスプレイ、例えばラップトップコンピュータの普及にともなって、さまざまなプレイ技術、例えば液晶ディスプレイ（ＬＣＤ）および発光ダイオードディスプレイ（ＬＥＤ）が使用されるようになった。一般的に、ポータブルディスプレイにおいては、ディスプレイを使用するポータブルシステムの電力を節約し、それによってポータブルシステムの「使用時間」を延長できる様にすることが重要である。

【０００４】ＬＣＤにおいては、ディスプレイの使用中の全期間にわたってバックライトがオンになっている。すなわち、ＬＣＤ内のすべての画素が点灯され、ある画素を「暗く」するには、画素を通る光を偏光層でさえぎる。これに対して、ＬＥＤディスプレイは、通電された画素のみが点灯され、暗い画素を点灯する必要をなくして省電力を図っている。

【０００５】図２に、２個のＮＭＯＳトランジスタＮ１とＮ２を有する従来技術のアクティブマトリックスＬＥＤ画素構造２００を示す。この画素構造においては、トランジスタＮ１に通電することによりコンデンサＣにデータ（電圧）が先ず保存され、次に「駆動トランジスタ」Ｎ２に通電してＬＥＤを点灯する。画素構造２００を使用したディスプレイでも節電は可能であるが、この画素構造では、いくつかの原因により不均一な輝度レベルを呈する。

【０００６】第一に、ＬＥＤの輝度はそこを通る電流に比例することが観測されている。使用中、「駆動トランジスタ」Ｎ２の閾値電圧がドリフトするためＬＥＤを通

る電流が変化する可能性がある。この電流の変化がディスプレイの輝度の不均一性の一因となる。

【０００７】第二に、ディスプレイの輝度の不均一性のもう一つの原因は、「駆動トランジスタ」Ｎ２の製造において見いだすことが出来る。いくつかの場合に、「駆動トランジスタ」Ｎ２は、トランジスタの初期閾値電圧の均一性の確保が困難な材料で作られ、その結果、画素ごとに変動する。

【０００８】第三に、ＬＥＤの電気的パラメータも不均一性を呈することがある。例えば、バイアス温度ストレス条件下では、ＯＬＥＤ（有機発光ダイオード）のターンオン電圧の増加が予想される。

【０００９】従って、画素構造の「駆動トランジスタ」における閾値電圧の変動に起因する電流の不均一性を低減する画素構造と、それに関連する方法が当該技術分野において必要となっている。

【００１０】

【発明が解決しようとする課題】本発明は、画素構造の発光ダイオードにおける電流の不均一性の低減によって輝度の均一性を改善するＬＥＤ（またはＯＬＥＤ）画素構造と方法を提供することを目的とする。

【００１１】

【課題を解決するための手段】上記課題を解決するために、本発明者らは鋭意検討した結果、５個のＮＭＯＳトランジスタ、コンデンサ、およびＬＥＤから成る画素構造が上記課題を解決できることを見出し、本発明を完成するに至った。

【００１２】すなわち、本発明の第一の要旨は、少なくとも一つの画素を備えるディスプレイであって、当該画素は、（１）第１選択ラインへの接続用であるゲートと、ソースと、ドレインとを有する第１トランジスタと、（２）当該第１トランジスタのドレインが接続されている第１端子と、第２端子とを有するキャパシタと（３）オートゼロラインへの接続用であるゲートと、ソースと、当該第１トランジスタの当該ドレインが接続されているドレインとを有する第２トランジスタと、（４）第２選択ラインへの接続用であるゲートと、当該第２トランジスタのドレインに接続されたソースと、ドレインとを有する第３トランジスタと、（５）当該第１トランジスタのソースに接続されたゲートと、ソースと、当該第２トランジスタの当該ソースに接続されたドレインとを有する第４トランジスタと、（６）当該第１トランジスタのソースに接続されたゲートと、ソースと、当該第３トランジスタの当該ドレインに接続されたドレインとを有する第５トランジスタと、（７）当該第４トランジスタのソースと当該第５トランジスタのソースとが、一方の端子に接続されている２個の端子を有する光要素とから成ることを特徴とするディスプレイに存する。

【００１３】第１の要旨の好ましい態様において、画素構造は３個のトランジスタと１個のダイオードから成る。

【００１４】第１の要旨の他の好ましい態様において、画素構造は５個のトランジスタを有する異なる画素構造である。

【００１５】第１の要旨の他の好ましい態様において、画素構造はオートゼロ化電圧範囲を拡張する追加のラインを１本備える。

【００１６】本発明の第２の要旨は、画素パラメータを測定し、それを使用して入力画素データを調節する、一つの外部測定モジュールと種々の測定方法に存する。

【００１７】

【発明の実施の形態】以下、本発明を図面を使用して詳しく説明する。尚、理解を容易にするため、各図に共通の要素は可能な限り同一の符号を付した。

【００１８】図３は、本発明によるアクティブマトリックスＬＥＤ画素構造３００の略図である。好ましい実施態様において、アクティブマトリックスＬＥＤ画素構造は、薄膜トランジスタ（ＴＦＴ）、すなわちポリシリコンまたはアモルファスシリコンを使用して作られたトランジスタを使用して実施される。同様に、好ましい実施態様において、アクティブマトリックスＬＥＤ画素構造は、有機発光ダイオード（ＯＬＥＤ）を使用する。この画素構造は薄膜トランジスタと有機発光ダイオードを使用して実施しているが、本発明は他のタイプのトランジスタや発光ダイオードを使用しても実施できる。

【００１９】この画素構造３００は、トランジスタ閾値電圧（V_t）の不均一性が大きくかつＯＬＥＤターンオン電圧の不均一性が大きい場合でも、均一な電流駆動を提供する。すなわち、ＯＬＥＤを通る電流を均一に保ち、それによってディスプレイの輝度の均一性を確保することが望ましい。

【００２０】図３を参照すると、画素構造３００は、５個のＮＭＯＳトランジスタＮ１（３１０）、Ｎ２（３２０）、Ｎ３（３３０）、Ｎ４（３４０）およびＮ５（３５０）、コンデンサ３０２、およびＬＥＤ（ＯＬＥＤ）（光要素）３０４（光要素）から成る。選択ライン３７０はトランジスタ３５０のゲートに接続されている。データライン３６０はコンデンサ３０２の一方の端子に接続されている。オートゼロライン３８０はトランジスタ３４０のゲートに接続されている。ＶＤＤライン３９０がトランジスタ３２０、３３０のドレインに接続されている。画素アレイ内の前の行からのオートゼロライン３８２が、トランジスタ３３０のゲートに接続されている。

【００２１】前行からのオートゼロライン３８２は第２の選択ラインとして実施可能であることに注目すべきである。すなわち、現在の画素のタイミングは、前行からのオートゼロライン３８２が第２の選択ラインを必要とせずに利用でき、それによって現在の画素の複雑さとコ

ストを低減するようになっている。

【００２２】コンデンサ３０２の一つの端子は（ノードＡにおいて）トランジスタ３３０のソースと、トランジスタ３４０、３５０のドレインに接続されている。トランジスタ３５０のソースは（ノードＢにおいて）トランジスタ３１０と３２０のゲートに接続されている。トランジスタ３１０のドレインはトランジスタ３４０のソースに接続されている。最後に、トランジスタ３１０と３２０のソースはＬＥＤ３０４の一方の端子に接続されている。

【００２３】前述のように、有機ＬＥＤディスプレイの駆動には種々の不均一性による問題が多い。本発明は、これらの問題を対象とする有機ＬＥＤディスプレイの構造に関する。すなわち、各ＬＥＤ画素は、ＬＥＤターンオン電圧の変動やＴＦＴ閾値電圧の変動に鈍感な方法で駆動される。すなわち、現在の画素は、ＬＥＤターンオン電圧やＴＦＴ閾値電圧の変動に対処するために使用されるオートゼロ化方法を使用して、オフセット電圧パラメータを求めることが出来る。

【００２４】更に、従来のアクティブマトリックス液晶ディスプレイにおいて使用された方法に極めて類似する方法によって、各画素にデータがデータ電圧として供給される。その結果、本発明のディスプレイ構造は、従来の行と列のスキャナに対し、外付けでも内蔵でも使用することが出来る。

【００２５】本発明の画素は、５個のＴＦＴと、１個のコンデンサと、ＬＥＤとを使用する。ＴＦＴの接続は、ＬＥＤのカソードにではなく、アノードに接続されることに注目すべきであり、このことは従来の有機ＬＥＤにおいてはＩＴＯがホールエミッタであるという事実によって必要とされる。従って、ＬＥＤはＴＦＴのドレインにではなく、ソースに接続される。各ディスプレイの列は、２本の行ライン（オートゼロラインと選択ライン）と、１－１／２列ライン（データラインと、隣の列と共有する＋ＶＤＤライン）を有する。各ライン上の波形も図４に示す。画素３００の作動を以下３フェーズ、すなわち３段階で詳述する。

【００２６】第一フェーズはプリチャージフェーズである。前行３８２のオートゼロ（ＡＺ）ライン上の正のパルスがトランジスタ３３０を「オン」にし、画素のノードＡをV_{dd}、例えば＋１０Ｖまでプリチャージする。次にデータラインが、前行の画素へデータを書き込むため、そのベースライン値から変化し、そのベースラインへ戻る。これは考慮中の画素への正味効果を持たない。

【００２７】第二フェーズはオートゼロフェーズである。現在の行のＡＺラインとＳＥＬＥＣＴラインが高くなり、トランジスタ３４０、３５０を「オン」にし、トランジスタＮ１　３１０のゲートを落とし、ターンオン電圧へと自己バイアスをかけ、ＬＥＤに極くわずかな電流を流す。このフェーズにおいて、ＬＥＤのターンオン電圧とＮ１の閾値電圧の合計がＮ１のゲートに保存される。Ｎ１とＮ２とはごく接近して配置できるので、それらの初期閾値電圧は極めて類似している。更に、これら２個のトランジスタのソースに対するゲート電圧V_{gs}は同じはずである。ＴＦＴの閾値電圧のドリフトはＴＦＴの全寿命にわたってV_{gs}のみに依存するので、これらデバイスの閾値電圧はＴＦＴの全寿命にわたって追従すると見なすことが出来る。従って、Ｎ２の閾値電圧もそのゲート上に保存される。オートゼロ化の完了後、オートゼロラインはロー（low）に戻る一方、選択ラインはハイ（high）のままである。

【００２８】第三フェーズはデータ書き込みフェーズである。データはベースライン電圧を超える電圧としてデータラインへ印加され、コンデンサを介して画素に書き込まれる。次に選択ラインがローに戻り、データ電圧、プラスＬＥＤターンオン電圧、プラスＮ２の閾値電圧の合計が、残りのフレームに関してノードＢに保存される。保存されたデータがリークによって失われないように、ノードＢから＋V_{dd}までのコンデンサを使用できることに注目すべきである。

【００２９】要するに、オートゼロフェーズの間、細電流（trickle current）を使用して、ＬＥＤのターンオン電圧とＮ２の閾値電圧が「測定」され、ノードＢに保存される。このオートゼロフェーズは、本質的には駆動電流が極めて小さい電流駆動モードの作動である。オートゼロフェーズの後の書き込みフェーズになって初めて、印加されたデータ電圧を使用してＬＥＤに増分が与えられる。従って、本発明は、電圧駆動または電流駆動よりはむしろ、「ハイブリッド駆動」を有するということが出来る。ハイブリッド駆動方法は、電圧駆動および電流駆動における欠点がなく、両者の長所を組み合わせるものである。ＬＥＤのターンオン電圧とＴＦＴの閾値電圧の変動は、電流駆動における場合と全く同様に補正される。同時に、ディスプレイ上のすべてのラインは電圧によって駆動されるので、高速で駆動することが出来る。

【００３０】注目べきことに、データライン３６０に印加されるデータ電圧の増分は、ＬＥＤ３０４全体にわたって直接現れるのではなく、Ｎ２（３２０）とＬＥＤのV_{gs}間に分割される。このことは単に、データ電圧からＬＥＤ電圧への非線型のマッピングがあることを意味する。このマッピングは、ＬＥＤ電圧からＬＥＤ電流への非線型のマッピングと組み合わされて、データ電圧からＬＥＤ電圧への全体の伝達関数を発生するが、これは単調で、上記のようにディスプレイの全寿命にわたって安定している。

【００３１】現在の画素構造３００の利点は、閾値が補正されない画素におけるトランジスタ（Ｎ３、Ｎ４およびＮ５）がフレームあたり１列時間のみオンとなるためデューティサイクルが極めて短く、認識できるほどには

シフトしないと予想されることである。更に、Ｎ２は、ＬＥＤの現在パスにおける唯一のトランジスタである。このパス上で直列接続されたトランジスタは、ディスプレイ効率を劣化させるか、あるいは未補正のＴＦＴ閾値シフトによる問題を発生する可能性があり、もしも一つの列上の全部の画素によって共有されると、縦方向の著しいクロストークをもたらす可能性がある。

【００３２】選択パルスとオートゼロ（ＡＺ）パルスは行スキャナによって形成される。列データはＡＺパルス同士間のタイムスロットにおいて（任意の）一定ベースライン電圧に加えて印加される。選択信号の下降エッジは、データライン上でデータが有効である間に発生する。直接サンプル・タイプまたはチョップト・ランプ・タイプのいずれかの各種の外付けまたは内蔵の列スキャナが、このタイミングによってデータを発生することが出来る。

【００３３】上記の画素構造によれば、有機ＬＥＤを使用して大型の直視ディスプレイを造ることが出来る。もちろん、現在の画素構造は、駆動電流を必要とするディスプレイ要素を使用する任意のディスプレイ技術にも、特にディスプレイ要素またはＴＦＴのターンオン電圧がシフトするかまたは不均一である場合、適用可能である。

【００３４】図５は、本発明によるアクティブマトリックスＬＥＤ画素構造５００の好ましい実施態様の略図である。この画素構造５００は、図３の画素構造３００に類似であるが、ここでは２個のトランジスタの代わりにショットキダイオード１個を使用している。

【００３５】画素構造３００が有する可能性のある欠点の一つとして、１画素あたり５個のトランジスタを使用していることが挙げられる。すなわち、各画素に多数のトランジスタを使用しているので、画素のフィルファクタ（fill factor）（アクティブプレートを通るボトム側放出を想定して）およびその収率（yield）にも影響を及ぼす可能性がある。従って、画素構造３００は、各画素に１個のショットキダイオードのみを使用してトランジスタ数を５個から３個に減らしつつ、且つ上記と同じ機能を果たす。

【００３６】図５において、画素５００は３個のＮＭＯＳトランジスタＮ１（５１０）、Ｎ２（５２０）、Ｎ３（５３０）、１個のコンデンサ５０２、１個のショットキダイオード５４０、およびＬＥＤ（ＯＬＥＤ）５５０（光要素）から成る。選択ライン５７０はトランジスタ５３０のゲートに接続されている。データライン５６０はコンデンサ５０２の一方の端子に接続されている。オートゼロライン５８０はトランジスタ５２０のゲートに接続されている。点灯ライン（ＶＤＤラインに類似）５９０はショットキダイオード５４０の一方の端子に接続されている。

【００３７】コンデンサ５０２の一方の端子は（ノードＡにおいて）トランジスタ５２０と５３０のドレインに接続されている。トランジスタ５３０のソースは（ノードＢにおいて）トランジスタ５１０のゲートに接続されている。トランジスタ５１０のドレインはトランジスタ５２０のソースと、ショットキダイオード５４０の一方の端子に接続されている。

【００３８】画素構造５００も、下記のように、プリチャージフェーズ、オートゼロフェーズ、およびデータ書き込みフェーズの３フェーズで作動する。すべての点灯ラインはディスプレイの周囲で相互に結合されていて、プリチャージフェーズが始まる前に、これら点灯ラインは、約＋１５Ｖのプラスの電圧V_{ILL}に保持される。以下の説明においては、考慮中の行を「行ｉ」と呼ぶ。各ライン上の波形も図６に示す。

【００３９】第一フェーズはプリチャージフェーズである。プリチャージは、オートゼロ（ＡＺ）ラインがトランジスタＮ２をオンにし、選択ラインがトランジスタＮ３をオンにすると開始される。このフェーズは、データラインがリセットレベルにあるとき行なわれる。ノードＡとＢにおける電圧はトランジスタＮ１のドレインと同じ電圧まで上昇するが、これはV_{ILL}より低いダイオード降下である。

【００４０】第二フェーズはオートゼロフェーズである。次に、点灯ラインがアースに落ちる。このフェーズ中、アレイ上のすべての画素は短時間暗くなる。ここで、ショットキダイオード５４０がトランジスタＮ１のドレインを、アースされた点灯ラインから絶縁して、Ｎ１のオートゼロ化が始まる。ノードＢがトランジスタＮ１の閾値電圧プラスＬＥＤ５５０のターンオン電圧にほぼ等しい電圧に達すると、ＡＺラインを使用してトランジスタＮ２を「オフ」にし、点灯ラインはV_{ILL}に戻る。選択されなかった行のすべての画素が再び点灯する。

【００４１】第三フェーズはデータ書き込みフェーズである。次に、行ｉに関するデータがデータラインに印加される。ノードＡとＢにおける電圧上昇が、データラインのリセット電圧レベルとデータ電圧レベル間の差を等しくする。このようにして、トランジスタＮ１の閾値電圧とＬＥＤのターンオン電圧の変動が補正される。ノードＢにおける電圧が落ち着いた後、行ｉに関する選択ラインを使用してトランジスタＮ３をオフにし、データラインがリセットされる。これで次のフレームまで適切なデータ電圧が画素に保存される。

【００４２】以上、先に述べた５トランジスタ画素の利点を持ちつつも、トランジスタ数の少ない、ＯＬＥＤディスプレイ用３トランジスタ画素について説明した。更なる利点として、５トランジスタ画素には、オートゼロ化とＬＥＤ駆動とに別々のトランジスタを使用されることである。画素３００が適切に作動するには、これら２個のトランジスタの初期閾値が一致し、寿命の全期間に

わたって同じようにドリフトすることが必要である。最近の実験データが示唆するところによれば、（これらトランジスタのように）ＴＦＴ同士のドレイン電圧が互いに異なると、両ＴＦＴは同様にはドリフトしない。従って、画素５００は、適切なオートゼロ化が保証されるように、ＬＥＤを駆動する同じトランジスタ上でオートゼロ化を行なう。

【００４３】図７は、本発明によるアクティブマトリックスＬＥＤ画素構造７００の代替実施態様の略図である。この画素構造７００は、図３の画素構造３００に類似するが、更に正確なオートゼロ電圧を発生する。

【００４４】すなわち、図３において、オートゼロ化は、各プリチャージサイクルが図３に示すように大きなプラス電荷Q_{PC}を画素３００のノードＡに注入するという事実から生ずる。プリチャージフェーズ中、ノードＡ上のキャパシタンスのほとんどすべてはコンデンサC_{data}からであり、ノードＡに注入される電荷は式（１）で表される。

【００４５】

【数１】

$$Q_{pc} \cong C_{data}(V_{DD} - V_A) \qquad (1)$$

【００４６】ここでV_Aは、プリチャージフェーズが始まる前のノードＡにおける電圧である。V_Aは、画素３００に予め与えられたデータ、Ｎ３（３００）の閾値電圧、およびＬＥＤ３０４のターンオン電圧に左右される。C_{data}が大きなキャパシタンス（約１ｐＦ）であるので、Q_{PC}も１０ピコクーロン（picocoulomb）程度と大きい。

【００４７】画素３００が安定したオートゼロレベルにあるとき、Q_{PC}はオートゼロフェーズ中、Ｎ１（３００）とＬＥＤ３０４とを通って流れる。オートゼロ間隔（インタバル）は短いので（約１０μsec）、Ｎ１にはその閾値電圧より高いゲート対ソースオートゼロ電圧が残る可能性があり、同様にＬＥＤもそのターンオン電圧を上回ってオートゼロ化する。このように、オートゼロ化プロセスにおいては、ノードＡとノードＢで、真のゼロ電流オートゼロ電圧ではなく、その近似値を発生する可能性がある。

【００４８】注目すべきことは、Ｎ１とＬＥＤを通る正確なゼロ電流に対応する真のゼロ電流オートゼロ電圧を発生させる必要がないという点である。本発明において、微弱な電流（約１０ナノアンペア）をＮ１ ３００とＬＥＤ ３０４とを通って流すことの出来るオートゼロ電圧を得ることが望ましい。オートゼロ間隔（インタバル）は約１０μsecであるので、Q_{PC}は約０．１ピコクーロン程度のはずである。上記のように、Q_{PC}は約１０ピコクーロンである。

【００４９】このように大きなQ_{PC}の効果として、画素の安定オートゼロ電圧が閾値電圧とターンオン電圧の合計をはるかに上回る可能性がある。この状態そのものは、もしも過剰なオートゼロ電圧がディスプレイ全体にわたって均一であれば、問題にはならない。すなわち、すべてのデータ電圧を相応にオフセットすることによって、この効果に対処することが出来る。

【００５０】しかし、もしもQ_{PC}が大きいのみならず、前のデータ電圧とオートゼロ電圧そのものに左右される場合、問題を生ずる可能性がある。この状態がもしもディスプレイ内で発生すると、すべての画素のオートゼロ電圧が大幅に過剰になるのみならず、過剰電圧の大きさが画素ごとに異なる可能性がある。実際、そのような条件下では、画素３００のオートゼロ化によって均一なディスプレイを作ることが出来ない。

【００５１】この問題に対処するため、画素７００はプリチャージQ_{PC}を極めて小さい値に下げることが出来る。また、オートゼロ化に実際に必要な電荷に応じてQ_{PC}を変化させることの出来る「可変プリチャージ」方法を開示する。要するに、現在のオートゼロ電圧が低すぎる場合、、オートゼロ電圧を所望の値にまで上げるため、Q_{PC}はその最小値、約０．１ピコクーロンとなる。しかし、現在のオートゼロ電圧が高すぎると、Q_{PC}は実質的にゼロになり、オートゼロ電圧が急速に下がることを可能にする。

【００５２】図７を参照すると、画素７００は、５個のＮＭＯＳトランジスタ、Ｎ１（７１０）、Ｎ２（７２０）、Ｎ３（７３０）、Ｎ４（７４０）、Ｎ５（７５０）と、コンデンサ７０２と、ＬＥＤ（ＯＬＥＤ）７０４（光要素）とから成る。選択ライン７７０はトランジスタ７１０のゲートに接続されている。データライン７６０はコンデンサ７０２の一方の端子に接続されている。オートゼロライン７８０はトランジスタ７４０のゲートに接続されている。ＶＤＤライン７９０はトランジスタ７２０と７５０のドレインに接続されている。画素アレイ内の前の行からのオートゼロライン７８２はトランジスタ７５０のゲートに接続されている。

【００５３】本発明において、前の行からのオートゼロラインを第二選択ラインとすることが出来ることが特徴である。すなわち、現在の画素のタイミングを、第二選択ラインを必要とせずに前の行からのオートゼロライン７８２を利用できるようなタイミングにして、現在の画素の複雑さとコストを低減することが出来る。

【００５４】コンデンサ７０２の一方の端子は（ノードＡにおいて）トランジスタ７１０のドレインに接続されている。トランジスタ７１０のソースは（ノードＢにおいて）トランジスタ７２０、７３０のゲートに接続され、トランジスタ７４０のソースに接続されている。トランジスタ７４０のドレインは（ノードＣにおいて）トランジスタ７５０のソースとトランジスタ７３０のドレインに接続されている。最後に、トランジスタ７３０、７２０のソースはＬＥＤ７０４の一方の端子に接続され

ている。

【００５５】更に具体的に、画素７００は、トランジスタＮ３（７３０）のドレインであるノードＣにプリチャージ電圧が印加されること以外は、画素３００に類似する。更に、図８に示すようないくつかのタイミング変更もある。以下に、画素７００の作動を３フェーズの段階に分けて説明する。

【００５６】第一フェーズは前のラインタイム中、すなわちデータが前の行の画素に印加される前に行なわれるプリチャージフェーズである。選択ライン上のプラスのパルスがＮ１を「オン」にし、これによってノードＡとＢが互いにショートされ、画素７００の状態が、直前のオートゼロフェーズの後の状態に戻る。すなわち、画素は、画素の適切なオートゼロ電圧の最近の推測値である、データに依存しない電圧に戻る。Ｎ１が「オン」である間、前の行ラインからのオートゼロライン７８２上の正のパルスがトランジスタＮ５を「オン」にし、これによってノードＣをV_{dd}にプリチャージする。次に、トランジスタＮ１とＮ５が「オフ」とされる。

【００５７】トランジスタＮ１とＮ５のオン、オフの相対的タイミングは、あまり重要ではないが、トランジスタＮ１は、トランジスタＮ５がオフになる前にオンとしなければならない。そうしないと、トランジスタＮ３が旧データ電圧に応じて依然としてオンのままとなり、ノードＣへ注入された電荷がトランジスタＮ３を経てリークしてしまう可能性がある。

【００５８】プリチャージフェーズの後、電荷Q_{PC}はノードＣにおいて、トランジスタＮ３、Ｎ４、Ｎ５のゲート対ソース／ドレインのキャパシタンス上に保存される。これらキャパシタンスの合計は極めて小さく（約１０ｆＦ）、また、プリチャージ間隔がノードＣを約１０Ｖ上昇させるので、Q_{PC}は当初、約０．１ピコクーロンである。しかしこの電荷は、前のオートゼロ電圧の真のオートゼロ電圧に対する近似精度によって変化する割合で、オートゼロフェーズの前にノードＣからリークする。従って、オートゼロ化のためにはどれ程の電荷量が必要かということ次第で、$Q_{PC} \leqq$０．１ピコクーロンの関係はより精確に示されることになる。これは可変プリチャージ特徴である。直前のオートゼロ電圧が低すぎる場合、Ｎ３はプリチャージフェーズ後、非導通となり、Q_{PC}はその最大値に留まるはずであり、オートゼロフェーズ中、オートゼロ電圧をその要求レベルに向かって上昇させる。直前のオートゼロ電圧が高すぎる場合、Ｎ３は導通し、Q_{PC}はオートゼロフェーズが始まるまでにはリークし、オートゼロ電圧の急低下が可能になる。

【００５９】トランジスタＮ１とＮ５の相対的タイミングは重要ではないが、好ましいタイミングを図８に示す。プリチャージに要する時間を最短にするため、２個のトランジスタＮ１とＮ５は同時にオンとされる。Ｎ１はＮ５より前にオフとされるが、これにより、ノードＣからのQ_{PC}の（意図的な）リークは、Ｎ１をオフにすることによって容量的に押し下げられたノードＢ電圧に対応する。これにより、ノードＣからのQ_{PC}のリークは、画素にゼロデータが印加されたときに等しいノードＢ電圧に確実に対応する。

【００６０】要するに、画素７００は、画素３００に比してより効果的なオートゼロ化を可能にする画素のプリチャージ手段を提供する。具体的には、画素７００のオートゼロ化は、より正確、迅速、かつデータに対して独立性である。コンピュータシミュレーションによる確認では、画素７００は、オートゼロ化が良好であり、１０，０００時間の作動寿命の全期間にわたってほぼ一定のＯＬＥＤ電流対データ電圧特性を維持することが出来る。

【００６１】図９は、本発明の他の実施態様であるアクティブマトリックスＬＥＤ画素構造９００の略図である。画素構造９００は、図７の画素構造７００に類似しているが、追加の$V_{precharge}$ライン９９２を備え、ＬＥＤ供給電圧V_{dd}を上げずにオートゼロ電圧範囲を拡張することが出来る点が異なる。画素のこの追加修正は、画素の寿命と効率を改善する。

【００６２】以上説明した画素（２００、３００、７００）は、V_{dd}がプリチャージ電圧であるので、オートゼロ電圧がV_{dd}を超えることが出来ないという制限がある。しかし、トランジスタＮ２とＮ３の閾値電圧がトランジスタの寿命期間にわたってドリフトし、ＴＦＴドリフト電圧とＯＬＥＤターンオン電圧のドリフトを補正するため、オートゼロ電圧をV_{dd}より高くする必要が生じる点に到達する。オートゼロ電圧は、より高い電圧に到達することは出来ないので、ディスプレイの均一性は急速に劣化し、ディスプレイの有用寿命の終りを告げる。V_{dd}を高くすれば、より高いオートゼロ電圧を達成できるが、V_{dd}はＯＬＥＤ駆動電源でもあるので、パワー効率が犠牲になる。

【００６３】更に、パワー効率の改善のため、V_{dd}を下げてトランジスタＮ２をライン形領域で作動させると、オートゼロ電圧の範囲は更に制限される。（もちろん、そのようにすると飽和状態で作動させた場合よりＮ２を大きくする必要がある。）この場合、短時間の作動の後、オートゼロ電圧はV_{dd}より高いレベルに到達する必要があるので、駆動寿命は極めて短くなる。

【００６４】図９を参照すると、画素７００に、オートゼロ電圧に対する制限をなくし、それによってV_{dd}を十分に上回ることを可能にするオプションの変更が組込まれている。画素９００は、列ライン９９２が追加され、それがトランジスタ９５０のドレインに接続されている以外は、画素７００と同じである。

【００６５】列ライン９９２は、ＤＣ電圧$V_{precharge}$をすべての画素に運ぶため、アレイに追加されている。これらすべての列ラインは、ディスプレイの端で相互接

続されている。$V_{precharge}$をV_{dd}より高いレベルに上げることによって、画素９００は、$V_{precharge}$より高い電圧にプリチャージを行ない、オートゼロ化することが出来る。の高い値は、ディスプレイ効率にほとんど影響を及ぼさない。

【００６６】各$V_{precharge}$ライン９９２は、画素の隣接する列との共有が可能であることに注目すべきである。この$V_{precharge}$ラインはまた、行ラインとして走らせ、隣接する行との共有が可能である。

【００６７】要するに、オートゼロ電圧の範囲をV_{dd}を超えて拡張するため、追加の電圧ラインを備えたＯＬＥＤ画素を開示する。これによってＯＬＥＤ駆動トランジスタは、パワー効率上必要な低い電圧で、場合によってはライン形領域においてすら、オートゼロ電圧を制限することなく、作動することが出来る。従って、長い作動寿命と高効率が達成できる。この変更を画素７００について説明したが、最終的には、このオプション変更は、上記画素２００、３００を含み、それらに限らない他のオートゼロ画素構造にも実施可能である。

【００６８】上記各画素構造は、ＯＬＥＤディスプレイ用として、画素におけるトランジスタ閾値電圧変動とＯＬＥＤターンオン電圧変動が補正されるように設計されているが、これら画素構造は、画素の外部で発生する不均一性に対処するようには設計されていない。この画素は、ディスプレイプレートの外部からでも、ディスプレイに一体化した状態でも、従来の列駆動回路に使用可能であることが指摘された。

【００６９】残念ながら、一体型データドライバは、外付けドライバほど精度がよくないのが普通である。市販の外付けドライバでは±１２ｍＶの精度を達成できるが、一体型ドライバでは±５０ｍＶの精度を達成できないことが判明している。一体型ドライバに特有なタイプの誤差は、オフセット誤差、すなわち、すべてのデータ電圧に加えられる、データ非依存性のＤＣレベルである。このオフセット誤差は不均一、すなわちＤＣレベルの値はデータドライバごとに変動する。液晶ディスプレイはオフセット誤差を許容する傾向がある。その理由は、フレームが順次反対極性で駆動され、あるフレームでオフセット誤差が液晶をわずかに暗くし、次のフレームで明るくするが、平均的にはほぼ正確で、交互の誤差は目で認識できないからである。しかし、ＯＬＥＤ画素は単一極性データによって駆動される。従って、オフセット誤差の二極消去は発生せず、一体型スキャナを使用すると深刻な不均一性問題が発生する可能性がある。

【００７０】図１０は、列トランジスタ１０２０を介してデータドライバ１０１０に接続された本発明のアクティブマトリックスＬＥＤ画素構造３００の略図である。本発明は、ＯＬＥＤディスプレイ用の一体型データスキャナにおけるオフセット誤差の消去方法を説明する。すなわち、この方法は、画素がデータラインに容量的に接続され、例えば上記の画素２００、３００、５００および７００のようなオートゼロフェーズを有する任意の画素とともに作動するように設計されている。

【００７１】図１０を参照すると、上記の画素３００は、ＯＬＥＤ要素の輝度を確定するため画素にアナログレベルを供給するデータラインに接続されている。図１０において、データラインは、データライン上に電圧を設定するためのチョップト・ランプ技法（chopped ramp technique）を使用するデータドライバによって駆動される。このアプローチ（技法）には、データライン上にオフセット誤差を発生させる種々の誤差源が存在する。例えば、電圧比較器が切り替わる時間は、比較器の最大スルーレート（slew rate）次第で変動する可能性がある。また、最大スルーレートは大幅に変動することが、実験によって観察されている。オフセット誤差は、画素に保存されている電圧に影響を及ぼす。オフセット誤差はまた、不均一であるので、ディスプレイ全体にわたって輝度の変動をもたらす。

【００７２】本発明においては、画素がそれ自体の内部閾値誤差を消去するためのオートゼロ化の期間を、データスキャナのオフセット誤差のキャリブレーションにも使用する。種々のラインの波形を図１１に示す。

【００７３】すなわち、これは実際のデータ電圧を印加するのと同じ列ドライバを使用してデータライン上に基準ブラックレベルを設定することによって達成される。画素のオートゼロフェーズ中に印加されるこの基準ブラックレベルは、実際のデータ電圧が設定されるのと全く同じやり方でデータライン上に設定される。すなわち、データランプ（data ramp）は電圧比較器によって定められる時間においてチョップされる。従って、画素のコンデンサＣを横切る電圧は画素のターンオン電圧と、ブラックレベルにオフセット誤差電圧をプラスした組合せによって定まる。基準ブラックレベルは、オートゼロフェーズの全期間、維持される。実際のデータが画素に印加されると、データスキャナオフセット誤差は画素のコンデンサ上に保存された電圧によって消去される。

【００７４】この技法は、チョップト・ランプを使用する一体型スキャナのみならず、列上へ直接サンプリングを使用するスキャナにも適用可能である。直接サンプリングの場合、誤差は、（大きな）列トランジスタがオフにされるとき、ゲート信号のデータラインへの不均一容量フィードスルーによって発生する。このトランジスタの閾値電圧変動は、チョップト・ランプ・データ・スキャナによって生じる不均一オフセット誤差と全く同様に、不均一オフセット誤差を生じる。

【００７５】従って、これは同様に補正できる。ブラック基準電圧は、画素のオートゼロフェーズ中、列に書き込まれる。一行のすべての画素が同時にオートゼロ化するので、このブラックレベルは、ラインタイム開始時にすべてのデータ列に同時に書き込まれる。ブラックレベ

ルはオートゼロフェーズの全期間中、維持される。チョップト・ランプ・スキャナの場合のように、実際のデータが画素に印加されると、オフセット誤差は画素キャパシタに保存されている電圧によって消去される。しかし、オフセット誤差の補正に必要な時間オーバーヘッドは、チョップト・ランプ技法を使用するよりも、直接サンプリング技法を使用する方が少ないように思われる。

【００７６】データドライバ誤差を補正するための本発明の方法は、別の方法よりも輝度の均一性のはるかに良好な有機ＬＥＤディスプレイの作成を可能にするはずである。ここに説明した方法と、上記いずれかのオートゼロ化画素を使用して、ディスプレイの全寿命にわたって均一性に目立った劣化のない、８ビットの輝度均一性が達成可能である。

【００７７】上記開示では、ディスプレイの輝度の不均一性に対処するため使用することの出来る複数の画素構造を記述したが、代替のアプローチ（技法）として、外付け手段によって不均一性を補正することが出来る。より具体的には、下記の開示は、ディスプレイの輝度の不均一性に対処するための方法と外付けキャリブレーション回路を説明する。要するに、すべての画素について不均一性を測定し保存し、測定した不均一性を使用して、データ（例えばデータ電圧）のキャリブレーションを行なうことが出来る。

【００７８】このように、以下の説明においては、図２の従来の画素構造を使用するが、本発明の外付けキャリブレーション回路と方法は、上記の画素３００、５００、７００を含み、これらに限らない他の画素構造にも使用することが出来る。しかし、本発明の外付けキャリブレーション回路と方法によって不均一性に対処すれば、より簡単な画素構造をディスプレイに採用でき、それによってディスプレイの収率とフィルファクタ（fill-factor）を増加させることが出来る。

【００７９】図１２は、画素２００のアレイ（集合）を相互接続して画素ブロック１２００とした状態の略図である。図２を参照すると、動作の際、データは、アクティブマトリックスディスプレイで普通に行なわれる方法で、画素アレイに書き込まれる。すなわち、選択ラインを高く駆動することによって画素の一行が選ばれ、それによってアクセストランジスタＮ１がオンとなる。各データラインにデータ電圧を印加することによって、この行の各画素にデータが書き込まれる。ノードＡにおける電圧が安定した後、選択ラインを低く駆動することによって、この行が選択から解除される。このデータ電圧は、次のフレームでこの行が選択されるまで、ノードＡに保存される。Ｎ１がオフにされている間に、ノードＡから多少の電荷リークの可能性があるので、不適当なレベルの電圧降下を防ぐため、ノードＡに蓄電コンデンサが必要になるかも知れない。図中の破線は、電圧降下に対処するための、コンデンサの接続方法を示す。しかし、そのような追加のコンデンサを不要にするほど十分なキャパシタンスがＮ２のゲートに関連して存在するかもしれない。

【００８０】注目すべきことに、ＯＬＥＤの輝度Ｌは、その電流Ｉにほぼ比例し、比例定数はディスプレイ全面にわたってかなり安定している。従って、良好に確定されたＯＬＥＤ電流を発生させれば、ディスプレイは視覚的に均一になる。

【００８１】しかし、プログラムによって画素へ供給されるのは、ＯＬＥＤ電流ではなくＮ２上のゲート電圧である。ＴＦＴ閾値電圧と相互コンダクタンス（transconductance）は、ＯＬＥＤの電気的パラメータが呈するように、ディスプレイ全体にわたる多少の初期不均一性を呈する可能性がある。更に、ＴＦＴ閾値電圧は、ＯＬＥＤターンオン電圧と同様に、バイアス温度ストレス条件下で増加することが周知である。従って、これらのパラメータは、当初不均一であり、各画素の個々のバイアス履歴に依存する態様で、画素の全寿命にわたって変化するものと期待される。これらパラメータを補正せずにＮ２のゲート電圧のプログラムを作成すると、ディスプレイは当初から不均一で、ディスプレイの全寿命にわたって不均一性が次第に増大する。

【００８２】本発明は、ＴＦＴとＯＬＥＤの電気的パラメータが補正され、それによって良好に確定されたＯＬＥＤ電流が画素アレイ内に生じるような方法である。Ｎ２に印加されるデータ電圧を補正するための方法を以下に説明する。

【００８３】図２と図１２は、データラインに並列に配置されたＶＤＤ供給ラインを有する画素アレイを示す。（好ましい実施態様において、ＶＤＤラインは選択ラインに並列に配線することが出来る。）このようにして、画素が２個またはそれ以上の隣接する列で各ＶＤＤラインを共有して、ＶＤＤラインの本数を減らすことが出来る。図１２は、ＶＤＤラインがディスプレイの周囲で結束されてブロック化された状態を示す。各画素ブロック１２００に含まれるＶＤＤラインの数は、１本と少なくても、ディスプレイ上のＶＤＤラインの全数のように多くてもよい。しかし、好ましい実施態様において、各画素ブロック１２００は、約２４本のＶＤＤライン、すなわち約４８の画素列を含む。

【００８４】図１３は、ディスプレイ１３１０とディスプレイコントローラ１３２０との相互接続の略図である。ディスプレイ１３１０は複数の画素ブロック１２００から成る。ディスプレイコントローラ１３２０は、ＶＤＤコントロールモジュール１３５０、測定モジュール１３３０、および種々のＩ／Ｏデバイス、例えばＡ／Ｄコンバータや、画素パラメータを保存するためのメモリーから成る。

【００８５】各画素ブロックは、図１２、１３に示すように、ディスプレイの端において検知ピン（ＶＤＤ／Ｓ

ＥＮＳＥ）１２１０に接続されている。通常のディスプレイ作動中、検知ピン１２１０は、例えば１０ないし１５ボルトの外部V_{dd}電源に切り替えられ、これによってＯＬＥＤエレメントを点灯するための電流をディスプレイに供給する。更に具体的には、各ＶＤＤ／ＳＥＮＳＥピン１２１０は、ディスプレイコントローラ１３２０において、一対のｐチャンネルトランジスタＰ１（１３５２）とＰ２（１３３２）および電流検知回路１３３４に接続されている。通常の作動中、ディスプレイコントローラからのＩＬＬＵＭＩＮＡＴＥ信号がＰ１を作動させてＶＤＤ／ＳＥＮＳＥピンをV_{dd}電源に接続する。典型的な実施態様において、Ｐ１を通る電流は約１ｍＡ／列と予想される。

【００８６】ＴＦＴとＯＬＥＤのパラメータを補正するため、特別測定サイクル中、各画素のパラメータに関する情報を収集するため、ＭＥＡＳＵＲＥ信号を介して外付け電流検知回路１３３４を作動させる。収集された情報は、通常のディスプレイ作動中、必要なＯＬＥＤ電流を実現するのに適したデータ電圧の計算および調整に使用される。

【００８７】更に具体的には、特定の画素の測定サイクル中、画素ブロック内の他のすべての画素は、それらに低いデータ電圧（例えばゼロ以下）を印加することによって、オフにされ、それによって、「オフ」画素からの電流の引き出しを確実に無視できるようにする。次に、対象とする画素によって引き出された電流が、１個以上の印加データ電圧に応じて測定される。各測定サイクル中、データパターン（すなわち、あるブロック中で、１個の画素のみがオンで、その他すべての画素がオフ）が、通常の方法で画素に印加され、データドライバ回路によってデータがＤＡＴＡラインに印加され、行が一つずつ選択される。このようにして、ディスプレイが複数の画素ブロックに区画されるので、各画素ブロック内の少なくとも１個の画素をオンにすることによって、複数の画素を測定することが出来る。

【００８８】各画素ブロック内の対象画素によって引き出された電流は、ＩＬＬＵＭＩＮＡＴＥラインとＭＥＡＳＵＲＥラインを、ＶＤＤ／ＳＥＮＳＥピン１２１０をＶＤＤ電源から切り離すとともに検知ピンをＰ２経由で電流検知回路１３３４のインプットに接続するレベルに駆動することによって外部からＰ２において測定される。画素電流は１ないし１０μＡと予想される。電流検知回路１３３４は図１３に相互インピーダンス増幅器として示してあるが、電流検知回路を他の形態で実施することも出来る。本発明においては、増幅器は入力端における電流に比例した電圧を出力端に発生する。この測定された情報は、Ｉ／Ｏデバイス１３４０によって収集され、そこでこの情報はディジタル形式に変換され、データ電圧のキャリブレーション用に保存される。電流検知回路１３３４内の抵抗器は約１メガオームである。

【００８９】複数の電流検知回路１３３４が画素ブロックと一対一の対応で示してあるが、マルチプレックサ（multi-plexer、不図示）を使用すれば、電流検知回路の数を減らすことが出来る。すなわち、複数のＶＤＤ／ＳＥＮＳＥピンを単一の電流検知回路１３３４に多重化することが出来る。極端な場合、単一の電流検知回路を全ディスプレイ用に使用することが出来る。ＶＤＤ／ＳＥＮＳＥピンをこのように検知回路に多重化すると、外付け回路の複雑さは低減できるが、ディスプレイ測定時間は長くなる。

【００９０】画素測定サイクルを行なうためには、通常のディスプレイ作動を中断しなければならないので、画素測定は、見る人を出来るだけ邪魔しないようにタイミングを図らねばならない。画素パラメータは徐々に変化するので、特定の画素を頻繁に測定する必要はなく、測定サイクルは長期間にわたって分散することが出来る。

【００９１】すべての画素を同時に測定する必要はないが、可変測定ラグ（遅延）に基づく不均一性を避けるためには、同時測定が有利である。これは、ディスプレイモジュールが「オン」または「オフ」されるとき、すべての画素を迅速に測定することによって達成可能である。ディスプレイモジュールが「オフ」のとき画素を測定すれば、通常の作動の邪魔にはならないが、長い「オフ」期間後、保存された画素パラメータはもはや均一性を保証しないかも知れないという欠点がある。しかし、中断しない電源が利用可能であれば（例えばスクリーンセイバーモードにおいて）、ディスプレイが（ユーザーの観点から）「オフ」である間に測定サイクルを周期的に行なうことが出来る。もちろん、ディスプレイモジュールが「オン」のときすべての画素の迅速測定を含まない任意のオプションでは、パワーが「オフ」のとき測定情報を保存するための不揮発性メモリーが利用可能であることが必要である。

【００９２】もしも画素測定情報が利用可能であれば、ディスプレイの不均一性の種々の原因を補正するため、データ電圧の補正またはキャリブレーションをディスプレイに適用することが出来る。例えば、トランジスタの閾値電圧変動とＯＬＥＤターンオン電圧変動に対処するため、データ電圧の補正を行なうことが出来る。従って、上記およびその他のディスプレイ不均一性を補正することの出来る複数の方法を以下に説明する。これらの方法を使用すれば、ディスプレイに数個の、そのうちのいくつかは大きな不均一性の原因があっても、均一な高画質ディスプレイを提供することが出来る。

【００９３】この補正方法を説明するため、ディスプレイには図２の画素構造を使用するものと仮定する。しかし、この補正方法は、他の任意の画素構造を使用したディスプレイにも適用できる。

【００９４】図２を参照すると、ノードＡに保存された電圧はＮ２のゲート電圧であり、従ってＮ２とＬＥＤと

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を通る電流を確定する。Ｎ２上の電圧を変化させることによって、ＬＥＤ電流を変化させることが出来る。Ｎ２上のゲート電圧とＬＥＤを通る電流との関係を考慮する。ゲート電圧V_gは、以下の式（２）の様に、Ｎ２のゲート対ソース電圧V_{gs}と、ＬＥＤを横切る電圧V_{diode}の二つに分割することが出来る。

【００９５】

【数２】

$$V_g = V_{gs} + V_{diode} \qquad (2)$$

【００９６】飽和状態のＭＯＳトランジスタのドレイン電流は以下の式（３）で表される。

【００９７】

【数３】

$$I = \frac{2}{k}(V_{gs} - V_t)^2 \qquad (3)$$

【００９８】ここで、ｋはデバイスの相互コンダクタンスパラメータ、V_tは閾値電圧である（ライン形領域における作動は下記参照）。従って、以下の式（４）が得られる。

【００９９】

【数４】

$$V_g = V_t + \sqrt{\frac{2I}{k}} + \sqrt[m]{\frac{I}{A}} \qquad (7)$$

【０１０６】ＯＬＥＤのＩ－Ｖ特性を表すため、他の関数形式を使用することも出来るが、上記の式によれば、ゲート電流とダイオード電流との間の異なる関数関係をもたらすことに注目すべきである。しかし、本発明は、上記のＯＬＥＤのＩ－Ｖ特性の詳細な関数形に限定されず、従って、任意のダイオード的特性に関して作動するように適応させることが出来る。

【０１０７】ＯＬＥＤの輝度Ｌは、その電流Ｉにほぼ比例し、比例定数は、ディスプレイ全面にわたって安定かつ均一である。良好に確定されたＯＬＥＤ電流を発生させることが出来れば、ディスプレイは視覚的に均一となる。しかし、以上説明したように、画素は電流Ｉではなく、電圧V_gを使用してプログラムされている。問題は、ＯＬＥＤのパラメータＡとｍの他に、ＴＦＴのパラメータV_tとｋがディスプレイ全面にわたって、ある程度の初期不均一性を呈するという点である。更に、V_tがバイアス温度ストレス条件下で増加することは周知である。ＯＬＥＤパラメータＡは、ＯＬＥＤのターンオン電圧に直接関連し、バイアスストレス下で減少することが知られている。ＯＬＥＤパラメータｍは、オーガニック・バンド・ギャップ内のトラップの分布に関連があり、ＯＬＥＤの全寿命にわたって変化する。従って、これらのパラメータは初期に不均一であり、各画素の個々のバイアス履歴に依存してディスプレイの全寿命にわたって変化するものと予想される。これらのパラメータの変動を補正せずにゲート電圧をプログラムすると、ディスプレイは初期に不均一で、その全寿命にわたって不均一性が増大する。

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$$V_{gs} = \sqrt{\frac{2I}{k}} + V_t \qquad (4)$$

＊【０１００】ＯＬＥＤを通る前向き電流は以下の式（５）で表される。

【０１０１】

【数５】

$$I = AV_{diode}^{m} \qquad (5)$$

【０１０２】ここで、Ａとｍは定数である（Burrows 他の J. Appl. Phys. 79(1996)参照）。従って、以下の式（６）が得られる。

【０１０３】

【数６】

$$V_{diode} = \sqrt[m]{\frac{I}{A}} \qquad (6)$$

【０１０４】従って、ゲート電流とダイオード電流との全体的関係は、以下の式（７）で表される。

【０１０５】

【数７】

【０１０８】実際に、不均一性の原因は他にもある。ゲート電圧V_gは、意図したデータ電圧V_{data}に必ずしも等しくない。むしろ、データドライバにおけるゲイン誤差とオフセット誤差、およびＮ１の選択解除から発生する（データ依存性の）フィードスルーが、これら二つの電圧に差異を生じさせる。これらの誤差原因も、不均一であり、かつ、ディスプレイの全寿命にわたって変動する。上記およびその他のゲイン誤差とオフセット誤差を、以下の式（８）で表す。

【０１０９】

【数８】

$$V_g = BV_{data} + V_0 \qquad (8)$$

【０１１０】ここで、ＢとV_0はそれぞれゲイン係数とオフセット電圧であり、ともに不均一であり得る。式（７）と（８）を組み合わせて整理すると以下の式（９）が得られる。

【０１１１】

【数９】

$$V_{data} = V_{off} + C\sqrt{I} + D\sqrt[m]{I} \qquad (9)$$

【０１１２】ここで、V_{off}、Ｃ、Ｄは前出のパラメータの組合せである。

【０１１３】本発明は、V_{off}、Ｃ、Ｄ、およびｍの変動を補正するため、意図する（入力）データ電圧を補正する種々の補正方法を提供し、それによって画素アレイ内における良好に確定されたＯＬＥＤ電流の発生を可能にする。パラメータV_{off}、Ｃ、Ｄ、およびｍの変動を補正するため、上記の外付け電流検知回路が、各画素に関する情報、すなわち単一の画素によって引き出された電流を外部から測定することが出来る。パラメータV_{off}、Ｃ、Ｄ、およびｍに関して測定された情報を使用して、本発明は、通常のディスプレイ作動中、必要なＯＬＥＤ電流を確定するため、式（９）に従って適切なデータ電圧V_{data}を計算する。

【０１１４】また、電流の測定値から４個のパラメータV_{off}、Ｃ、Ｄ、およびｍを正確に計算することは、コンピュータでは高価になり、複雑な繰り返し計算が必要になる。しかし、効果的な補正を維持しつつ計算の複雑さを低減する良好な近似を使用することが出来る。

【０１１５】好ましい実施態様において、上記のように４個ではなく、わずか２個のパラメータを使用して画素の不均一特性を表すことが出来る。式（９）の画素の電＊流電圧特性を参照すると、通常の点灯レベルにおいて、Ｎ２のV_{gs}に関するＣ$\sqrt{\ }$Ｉ項と、V_{diode}に関するＤ$\sqrt[m]{\ }$Ｉ項とは、ほぼ同じ大きさである。しかし、それらの画素電流への依存性は大きく異なる。ｍの値は約１０であるので、普通の点灯レベルにおいては、Ｄ$\sqrt[m]{\ }$ＩはＣ$\sqrt{\ }$Ｉに比してはるかに弱いＩの関数である。例えば、Ｉを１００倍に増加させると、Ｃ$\sqrt{\ }$Ｉは１０倍になるが、Ｄ$\sqrt[m]{\ }$Ｉは（ｍを１０と仮定すると）１．５８倍にしかならない。すなわち、普通の点灯電流レベルにおいては、ＯＬＥＤのＩ－Ｖ曲線はＴＦＴのＩ－V_{gs}曲線よりはるかに急勾配となる。

【０１１６】従って、普通の電流レベルにおいて、Ｄ$\sqrt[m]{\ }$Ｉは電流に対して独立であり、その画素ごとの変動は単に一つのオフセット誤差として処理可能であるという近似が行なわれる。この近似は多少の誤差を持ち込むが、ディスプレイ全体の外観は大幅には劣化しない。従って、かなりの精度で、すべてのディスプレイの不均一性を、オフセットとゲインの変動として処理することが出来る。従って、（９）式は以下の式（１０）の様に近似することが出来る。

【０１１７】

【数１０】

$$V_{data} = V_{offset} + C\sqrt{I} \qquad (10)$$

【０１１８】ここで、$V_{offset} = V_{off} + D\sqrt[m]{\ }$ＩはＤ$\sqrt[m]{\ }$Ｉを含み、$V_{offset}$とＣは画素ごとに変動する。

【０１１９】図１４は、全画素のパラメータの測定によってディスプレイを初期化する方法１４００のフローチャートである。方法１４００は、ステップ１４０５から始まり、ステップ１４１０に進み、そこで、画素ブロック内の対象とする画素以外のすべての画素に、「オフ」データ電圧を印加する。

【０１２０】ステップ１４２０において、対象とする特定の画素のV_{offset}とＣを求めるため、方法１４００は二つのデータ電圧（Ｖ１とＶ２）を印加し、各データ電圧について電流を測定する。

【０１２１】ステップ１４３０において、電流Ｉ１とＩ２の平方根が計算される。好ましい実施態様において、この計算のために平方根表が使用される。

【０１２２】ステップ１４４０において、V_{offset}とＣとが求められる。すなわち、二つの変数を求めるのに二つの式を使用することが出来る。次に、特定の対象画素の求められたV_{offset}とＣを記憶装置、例えばメモリーに保存する。全部の画素の測定が終ると、メモリーはアレイ内の各画素について二つのパラメータV_{offset}とＣとを保存している。これらの値は、後に式（１０）を使用してV_{data}のキャリブレーションまたは調整に使用することが出来る。方法１４００は次にステップ１４５５において終了する。

【０１２３】測定される画素を通る電流は、Ｄ$\sqrt[m]{\ }$Ｉが二つの測定点においてほぼ等しくなるように、十分に高くなければならないことに注目すべきである。この条件は、一方の測定を、システムが発生可能な最高データ電圧において行ない、次に他方の測定をわずかに低いデータ電圧において行なうことによって満足させ得ることが望ましい。

【０１２４】ディスプレイの初期化が行なわれると、ディスプレイモジュールに供給された生の入力ビデオデータを修正することが出来る。入力ビデオデータは、例えば（１）画素電圧、（２）ガンマ補正された画素輝度、または（３）画素電流といった種々のフォーマットで存在することが出来ることに注目すべきである。従って、入力ビデオデータのキャリブレーションまたは補正を行なうための、保存されたパラメータV_{offset}とＣの使用は、各特定のフォーマットに依存する。

【０１２５】図１５は、画素電圧を表す入力ビデオデータの修正方法１５００のフローチャートである。方法１５００は、ステップ１５０５から始まり、ステップ１５１０へ進み、そこで対象画素に関して保存されたパラメ

ータ、例えばV_{offset}とＣが取出される。

【０１２６】ステップ１５２０において、方法１５００は、入力ビデオデータのキャリブレーションを行なうため、取出したパラメータを印加する。より具体的には、入力ビデオデータにはバイアスがかかっていない、すなわち、ゼロボルトはゼロ輝度を表し、ゼロより大きいデータはゼロより大きい輝度レベルを表すものと期待される。従って、電圧は$C_0\sqrt{I}$に等しいと見なすことが出来る。ここで、Ｉは必要電流、C_0は定数、例えば典型的な値は１０３Ｖ／$\sqrt{A}$である。入力ビデオデータがディスプレイモジュールに入る際の画素変動を補正するため、各画素について$V_{offset} = V_{off} + C\sqrt{I}$を、保存された$V_{offset}$とＣに基づいて計算する。この計算は、ビデオデータにＣ／C_0を掛けることと、その結果にV_{offset}を加えることとから成る。C_0による除法は、ビデオデータV_{data}が既に一定の係数１／C_0によって縮小されていれば不要である。Ｃによる乗法は、ディジタルロジックで直接、またはルックアップテーブルを使用して行なうことが出来る。例えば、後者の場合、Ｃの各値は、ビデオデータの値がインデックスであるとともにテーブルエントリーが乗法の結果であるテーブルを指定する。（あるいは、ルックアップテーブル内の入力ビデオデータとＣの役割を逆にすることも出来る。）乗法が行なわれた後、ディジタルロジックによりV_{offset}の急速加算が行なわれる。

【０１２７】ステップ１５３０において、得られた電圧V_{data}、すなわち修正または調整された入力データは、画素アレイのデータドライバに送られる。方法１５００は次にステップ１５３５で終了する。

【０１２８】ガンマ補正された輝度データの場合、入力ビデオデータは、$L^{0.45}$に比例する。ここで、Ｌは輝度である。これは、ＣＲＴ輝度-電圧特性に関して予め補正されたビデオデータでは典型的である。$L^{0.45}=\sqrt{L}$であり、また、ＯＬＥＤ輝度はその電流に比例するので、データは$\sqrt{I}$に比例するものとして処理することが出来る。従って、計算は先に説明したゼロオフセット電圧に関する方法と同様な方法で行なうことが出来る。

【０１２９】図１６は、画素電流、すなわち輝度を表す入力ビデオデータの補正方法１６００のフローチャートである。方法１６００は、ステップ１６０５から始まり、ステップ１６１０に進み、そこで測定された電流の平方根の値が求められる。すなわち、方法１６００は、Ｉを表すビデオデータが$\sqrt{I}$を発生するように処理されねばならないこと以外は、上記の方法１５００と同じである。上記のように、この演算は、図１４に示すように、画素電流測定値から画素パラメータV_{offset}とＣを求めるのに必要な平方根の値を与える表を使用して行なうことが出来る。ここで再びこの表を使用してビデオデータから$\sqrt{I}$を発生させる。

【０１３０】次にデータ補正ステップ１６１０ないし１６４５は、ステップ１６３０において入力データにＣを掛け、次にV_{offset}を加えて補正されたデータ電圧を求めること以外は、上記の方法１５００と同一である。

【０１３１】あるいは、別の実施態様において、上記のように２個または４個のパラメータではなく、１個のみのパラメータを使用して画素の不均一特性を表すことが出来る。すなわち、単一のパラメータを使用して画素の不均一特性を表すようにして更に単純化を行なう。

【０１３２】更に具体的には、多くの場合、画素ごとのゲイン係数Ｃの変動は小さく、V_{offset}のみが不均一性の有意の原因として残る。これは、ＴＦＴ相互コンダクタンスパラメータｋと電圧ゲイン係数Ｂが均一のとき発生する。この場合、各画素のV_{offset}のみを求めれば十分である。そうすると、データ補正は乗法を行なわず（ゲイン係数が均一であると見なされるので）、オフセットパラメータの加算のみを行なう。

【０１３３】この単一パラメータ手法は、上記のオートゼロ化ＯＬＥＤ画素構造に類似である。この単一パラメータ補正方法は、コンピュータ費用を低減するとともに、満足すべきディスプレイ均一性を生み出すはずである。しかし、ディスプレイの均一性保持が非常に重要な特定のディスプレイの使用に於ては、コンピュータの複雑さと費用が増しても、上記の２個または４個パラメータ方法を使用することが出来る。

【０１３４】ここでも、単一パラメータ抽出とデータ補正に関して、ディスプレイ初期化プロセスはデータのフォーマット（形式）に左右される。単一パラメータ手法は、ビデオデータが、（１）画素電圧、（２）画素電流、および（３）ガンマ補正された画素輝度、を表す場合に、ディスプレイの初期化とビデオデータの補正に使用することが出来る。

【０１３５】図１７は、全画素のパラメータの測定によるディスプレイの初期化方法のフローチャートを示す。方法１７００は、ステップ１７０５から始まってステップ１７１０へ進み、そこで、画素ブロック内の対象画素以外のすべての画素に「オフ」データ電圧が印加される。　ステップ１７２０において、対象とする特定の画素に関するV_{offset}とＣを求めるため、方法１７００は、２個のデータ電圧（Ｖ１とＶ２）を印加し、各データ電圧ごとに電流を測定する。

【０１３６】ステップ１７３０において、電流Ｉ１とＩ２の平方根を計算する。好ましい実施態様において、この計算に平方根表を使用する。

【０１３７】Ｃの値は均一であると考えられるので、それは理想的には、ディスプレイ内の任意の場所で２点測定を行なうことによって、求め得ることに注目すべきである。しかしこれは、対象画素が異常であるかも知れないので、問題を有するかもしれない。従って、２点測定は、各画素ごとに行なわれる。

【０１３８】ステップ１７４０において、Ｃの平均値が

求められる。すなわち、各電流測定値に関する√Ｉを計算するための表を使用して、ディスプレイのＣの平均値が計算できる。

【０１３９】ステップ１７５０において、各画素の電流測定値から平均値Ｃを使用して、各画素のV_{offset}が求められる。このようにして、ディスプレイ全体にわたるＣの小変動がV_{offset}の計算によって部分的に補正される。上記理由により、各画素の電流の測定は、可能な最高データ電圧において測定することが望ましい。

【０１４０】最後にステップ１７６０において、各画素のV_{offset}が記憶装置、例えばメモリーに保存される。次に、方法１７００はステップ１７６５において終了する。

【０１４１】図１８は、画素電圧を表す入力ビデオデータの補正方法１８００のフローチャートである。方法１８００は、ステップ１８０５から始まり、ステップ１８１０へ進み、そこで、対象画素に関して保存されているパラメータV_{offset}を取り出す。

【０１４２】ステップ１８２０において、方法１８００は、取出したパラメータV_{offset}を使用して入力ビデオデータのキャリブレーションを行なう。より具体的には、保存されたV_{offset}の値に基づいて、各画素に関する$V_{data} = V_{offset} + V_{data}$の値を計算する。

【０１４３】ステップ１８３０において、得られたV_{data}、すなわち補正された、または調整された入力データは画素アレイのデータドライバへ送られる。方法１８００は次に、ステップ１８３５において終了する。

【０１４４】図１９は、ビデオデータが画素電流を表す状況に関する全画素のパラメータの測定によるディスプレイの初期化方法１９００のフローチャートである。方法１９００は上記方法１７００に酷似している。上記方法１７００との相違は、方法１９００が追加のステップ１９５０を取り入れて計算されたＣの平均値を使用して、ゼロ・オフセットデータ電圧対画素電流の表を作成する場合である。この点から先の初期化とデータ補正プロセスにおいては、この表を使用することにより、平方根演算を行わない。この表は、平方根関数より高い精度で、画素の電流-電圧特性を表すものと期待される。この表は次に、後で使用するため、記憶装置、例えばメモリーに保存される。次に、個々の画素電流測定値を、この表に入れるためのインデックスとして使用して、個々の画素オフセットV_{offset}を求める。

【０１４５】図２０は、画素電流、すなわち輝度を表す入力ビデオデータの補正方法２０００のフローチャート＊である。方法２０００は、ステップ２００５から始まり、ステップ２０１０へ進み、そこで現在対象とする画素のV_{offset}を記憶装置から取出す。

【０１４６】ステップ２０２０において、ゼロ・オフセットデータ電圧対画素電流の表を使用して入力ビデオデータ電流からゼロ・オフセットデータ電圧を求める。ステップ２０３０において、このゼロ・オフセットデータ電圧を、取出されたV_{offset}に加える。最後に、ステップ２０４０において、補正または調整された入力ビデオデータを画素アレイのデータドライバへ送る。

【０１４７】要するに、ビデオデータがディスプレイモジュールに導入されると、各電流に対応するゼロ・オフセットデータ電圧がＶ－Ｉ表内で検索される。次に、保存されている画素オフセットをゼロ・オフセット電圧に加算し、その結果がデータドライバへの入力となる。方法２０００は次にステップ２０４５において終了する。

【０１４８】図２１は、ビデオデータがガンマ補正された輝度データを表す状況に関する全画素のパラメータの測定によるディスプレイの初期化方法２１００のフローチャートである。方法２１００は、上記方法１９００に酷似している。方法２１００と上記方法１９００との相違は、ステップ２１５０において、計算されたＣの平均値を使用してゼロ・オフセットデータ電圧対画素電流の平方根の表を作成するときである。すなわち、ビデオデータは、√Ｉを表すものとして近似させることが出来る。従って、Ｃの平均値を使用してV_{data}対√Ｉのゼロ・オフセット表を作成し、この表をメモリーなどの記憶装置に保存する。

【０１４９】図２２は、ガンマ補正された輝度データを表す入力ビデオデータの補正方法２２００のフローチャートである。方法２２００は、上記方法２０００に酷似している。上記方法２０００との相違は、V_{data}対√Ｉのゼロ・オフセット表において発生する。従って、要するに、入ってくるビデオデータを使用してゼロ・オフセットデータ電圧を探し、保存された画素オフセットをこれらの電圧に加える。

【０１５０】上記説明において、ＯＬＥＤ駆動トランジスタＮ２が飽和状態で作動するものと見なしている。Ｎ２がライン形領域で作動するならば、類似の補正方法を使用することが出来る。その場合、画素の電流電圧特性は以下の式（１１）で表される。

【０１５１】

【数１１】

$$V_{data} = V_{off} + C(I)I + D\sqrt[m]{I} \qquad (11)$$

【０１５２】ここで、Ｃ（Ｉ）はＩの弱い関数である。ここでも、上記のように、オフセット項とゲイン係数のみを求めればよい程度に、電流が十分に高ければ、$D\sqrt[m]{I}$項をV_{off}項に含めることが出来る。しかし、オフセット電圧のみを不均一と見なす単一パラメータ近似は、ゲイン係数Ｃ（Ｉ）が不均一なＯＬＥＤパラメータＡとｍを含むので、上記の飽和の場合に関する単一パラメータ近似ほど精度がよいとは予想されない。従って、

Ｎ２がライン形領域で作動するならば、２個パラメータ補正方法の方が単一パラメータ補正方法よりもはるかに性能がよいと思われる。

【０１５３】図２３は、本発明の複数のアクティブマトリックスＬＥＤ画素構造３００、５００、または７００を備えたディスプレイ２３２０を使用したシステム２３００のブロックダイヤグラムである。システム２３００は、ディスプレイコントローラ２３１０とディスプレイ２３２０とから成る。

【０１５４】更に具体的には、ディスプレイコントローラは、中央処理装置ＣＰＵ（２３１２）、メモリー２３１４、および複数のＩ／Ｏ装置（例えばマウス、キーボード、磁気装置や光装置などの記憶装置、モデム、Ａ／Ｄコンバータ、上記の測定モジュール１３３０などの各種モジュール）を有する汎用コンピュータとすることが出来る。ディスプレイ２３２０を作動させるためのソフトウェア命令（例えば上記種々の方法）は、例えば記憶媒体からメモリー２３１４へロードし、ＣＰＵ２３１２によって実行することが出来る。従って、本発明のソフトウェア命令は、コンピュータで読むことの出来る媒体に保存することが出来る。

【０１５５】ディスプレイ２３２０は、画素インターフェイス２３２２と、複数の画素（画素構造３００、５００、または７００）とから成る。画素インターフェイス２３２２は画素３００、５００、または７００の駆動に必要な回路を含む。例えば、画素インターフェイス２３２２は、図１に示したようなマトリックス・アドレッシング・インターフェイスとすることが出来、また、オプションとして追加の上記の信号ライン／制御ラインを含むことが出来る。

【０１５６】従って、システム２３００は、ラップトップコンピュータとして実施することが出来る。あるいは、ディスプレイコントローラ２３１０は、マイクロコントローラとして、または特定用途の集積回路（ＡＳＩＣ）として、またはハードウェアとソフトウェア命令との組合せとして、実施することが出来る。要するに、システム２３００は、本発明を組込んだ大きなシステム内において実施することが出来る。

【０１５７】本発明を、ＮＭＯＳトランジスタを使用するものとして説明したが、本発明は、関連電圧が逆転したＰＭＯＳトランジスタを使用しても実現可能である。

【０１５８】以上、本発明の種々の実施態様を本明細書に示しかつ詳細に説明したが、本発明の要旨を超えない限りにおいて多くの態様を取り得ることが出来る。

【０１５９】

【発明の効果】本発明のディスプレイは輝度の均一性が大幅に改善されており、その工業的価値は高い。

【図面の簡単な説明】

【図１】マトリックスアドレッシングインターフェイスのブロック図

【図２】従来技術のアクティブマトリックスＬＥＤ画素構造の略図

【図３】本発明のアクティブマトリックスＬＥＤ画素構造の略図

【図４】図３のアクティブマトリックスＬＥＤ画素構造のためのタイミング図

【図５】本発明の代替実施態様のアクティブマトリックスＬＥＤ画素構造の略図

【図６】図５のアクティブマトリックスＬＥＤ画素構造のためのタイミング図

【図７】本発明の代替実施態様のアクティブマトリックスＬＥＤ画素構造の略図

【図８】図７のアクティブマトリックスＬＥＤ画素構造のためのタイミング図

【図９】本発明の代替実施態様のアクティブマトリックスＬＥＤ画素構造の略図

【図１０】本発明の代替実施態様のアクティブマトリックスＬＥＤ画素構造の略図

【図１１】図１０のアクティブマトリックスＬＥＤ画素構造のためのタイミング図

【図１２】画素アレイを相互接続して画素ブロックとした略図

【図１３】ディスプレイとディスプレイコントローラとの相互接続の略図

【図１４】全画素のパラメータの測定によってディスプレイを初期化する方法のフローチャート

【図１５】画素電圧を表す入力データの補正方法のフローチャート

【図１６】画素電流すなわち輝度を表す入力ビデオデータの補正方法のフローチャート

【図１７】ビデオデータが画素電圧を表す場合、全画素のパラメータの測定によってディスプレイを初期化する方法のフローチャート

【図１８】画素電圧を表す入力ビデオデータの補正方法のフローチャート

【図１９】ビデオデータが画素電流を表す場合、全画素のパラメータの測定によってディスプレイを初期化する方法のフローチャート

【図２０】画素電流すなわち輝度を表す入力ビデオデータの補正方法のフローチャート

【図２１】ビデオデータがガンマ補正された輝度データを表す場合、全画素のパラメータの測定によってディスプレイを初期化する方法のフローチャート

【図２２】ガンマ補正された輝度データで表された入力ビデオデータの補正方法のフローチャート

【図２３】本発明による複数のアクティブマトリックスＬＥＤ画素構造を有するディスプレイを使用したシステムのブロック図

【符号の説明】

１００：ディスプレイ

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１１０：列データ発生装置
１２０：行データ発生装置
１３０：行ライン
１６０：表示要素（画素）
２００：従来技術のアクティブマトリックスＬＥＤ画素構造
３００：本発明の画素構造
３０２：コンデンサ
３０４：ＬＥＤ（ＯＬＥＤ）（光要素）
３１０：第１トランジスタ
３２０：第２トランジスタ
３３０：第３トランジスタ
３４０：第４トランジスタ
３５０：第５トランジスタ
３６０：データライン
３７０：選択ライン
３８０：オートゼロライン
３８２：前の行からのオートゼロライン
３９０：ＶＤＤライン
５００：本発明の好ましい画素構造
５１０：第１トランジスタ
５２０：第２トランジスタ
５３０：第３トランジスタ
５０２：コンデンサ
５４０：ショットキダイオード
５５０：ＬＥＤ（ＯＬＥＤ）（光要素）
５７０：選択ライン
５６０：データライン
５８０：オートゼロライン
５９０：点灯ライン
７００：本発明の好ましい画素構造
７０２：コンデンサ
７０４：ＬＥＤ（ＯＬＥＤ）（光要素）

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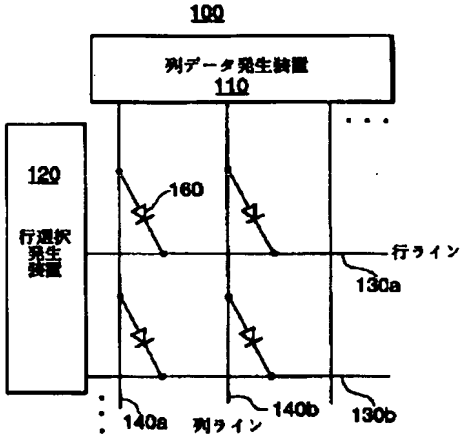
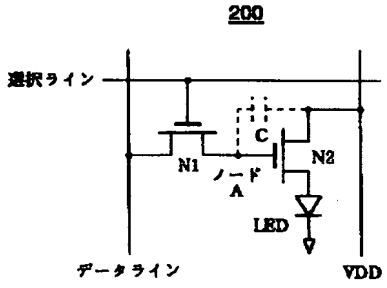
７１０：第１トランジスタ
７２０：第２トランジスタ
７３０：第３トランジスタ
７４０：第４トランジスタ
７５０：第５トランジスタ
７６０：データライン
７７０：選択ライン
７８０：オートゼロライン
７８２：前の行からのオートゼロライン
７９０：ＶＤＤライン
９００：本発明の好ましい画素構造
９９２：$V_{precharge}$
９５０：第５トランジスタ
１０００：本発明の画素構造
１０１０：データドライバ
１０２０：列トランジスタ
１２００：画素ブロック
１２１０：検知ピン（ＶＤＤ／ＳＥＮＳＥ）
１３１０：ディスプレイ
１３２０：ディスプレイコントローラ
１３３０：測定モジュール
１３３２：トランジスタＰ２
１３３４：電流検知回路
１３５０：ＶＤＤコントロールモジュール
１３５２：トランジスタＰ１
２３００：システム
２３１０：ディスプレイコントローラ
２３１２：中央処理装置ＣＰＵ
２３１４：メモリー
２３１６：Ｉ／Ｏ装置
２３２０：ディスプレイ
２３２２：画素インターフェイス

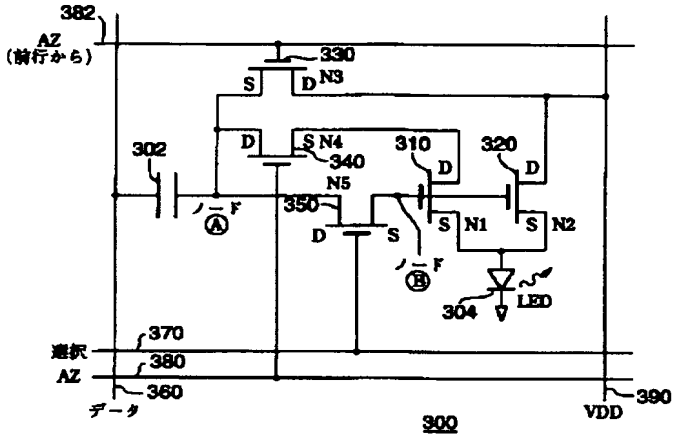
【図１】



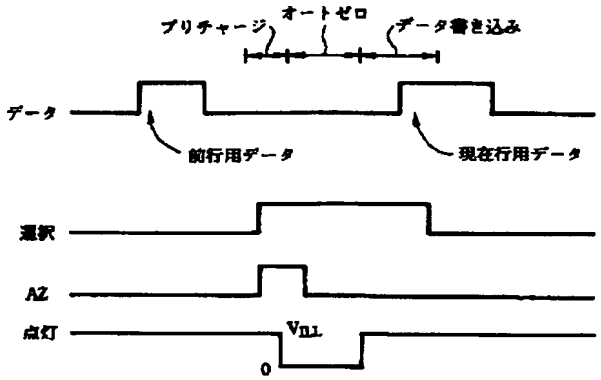
【図２】



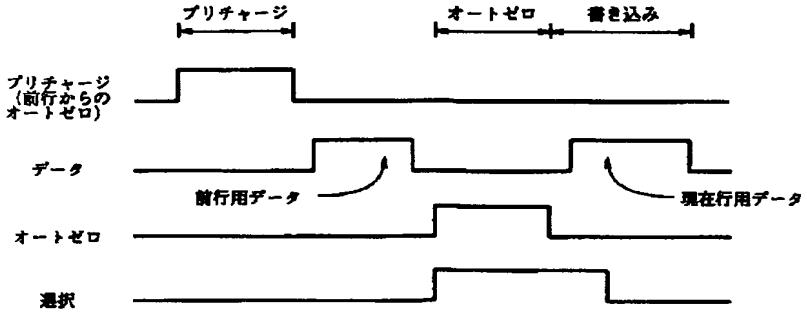
【図３】



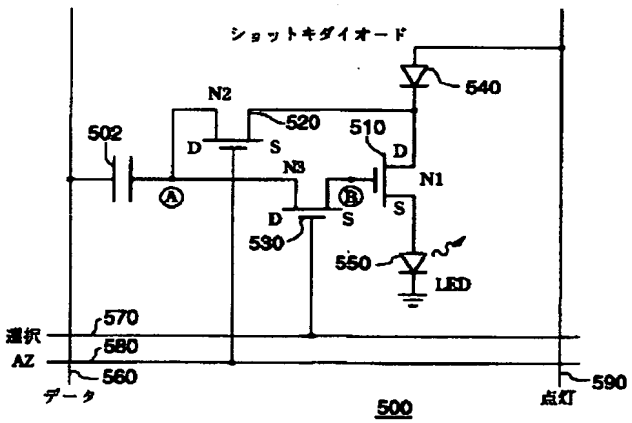
【図６】



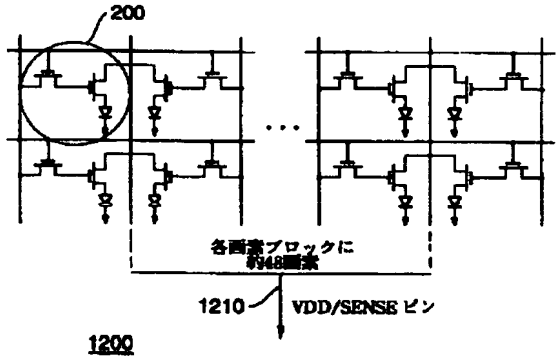
【図４】



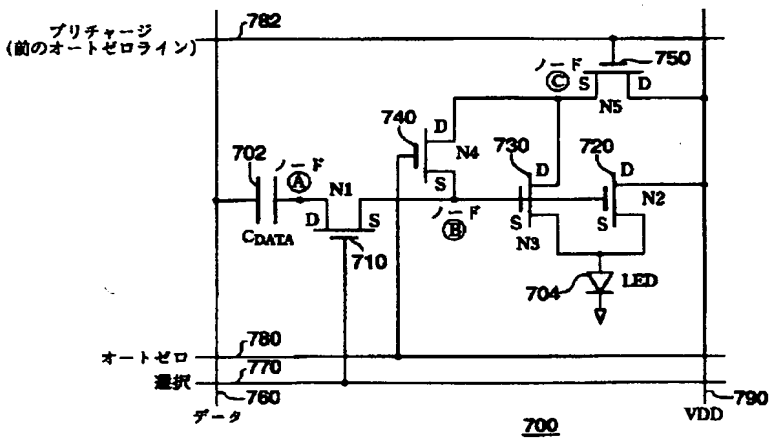
【図５】



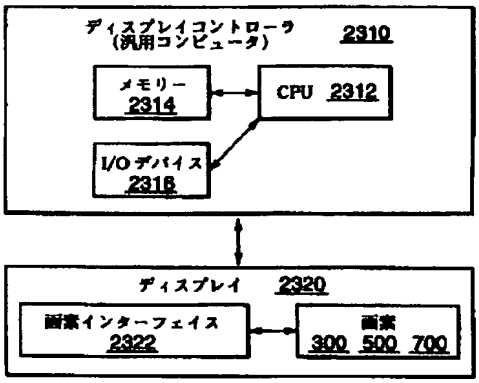
【図１２】



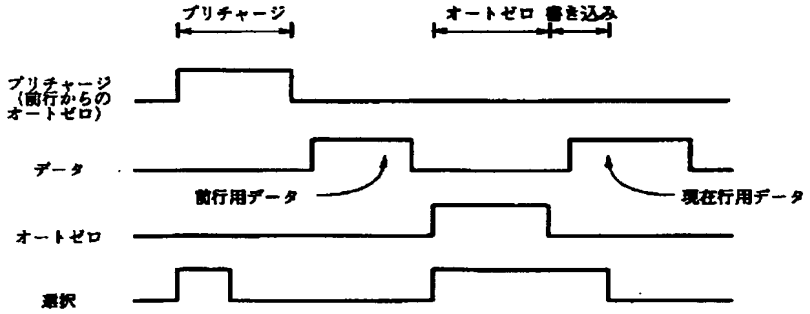
【図７】


プリチャージ
(前のオートゼロライン)
782
ノード
Ⓒ
750
S
D
N5
740
D
N4
730
D
720
D
702
ノード
Ⓐ
N1
N2
S
D
S
S
S
CDATA
710
ノード
Ⓑ
N3
704
LED
オートゼロ
780
選択
770
データ
760
790
VDD
700

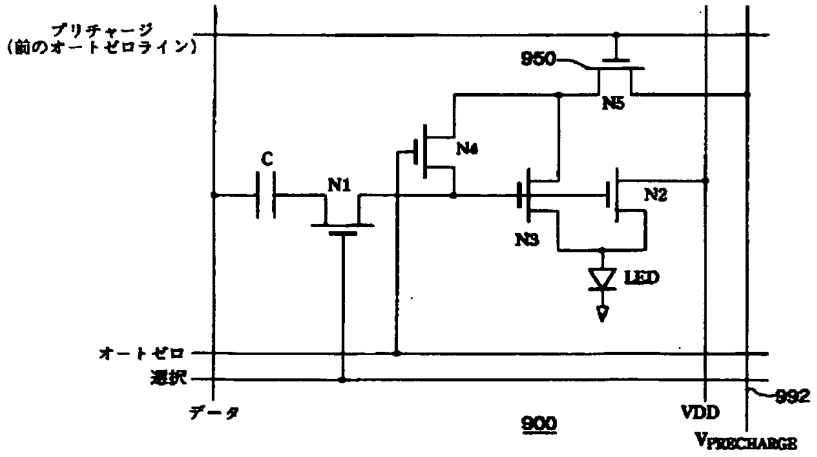
【図２３】


ディスプレイコントローラ
(汎用コンピュータ)
2310
メモリー
2314
CPU 2312
I/Oデバイス
2318
ディスプレイ
2320
画素インターフェイス
2322
画素
300 500 700

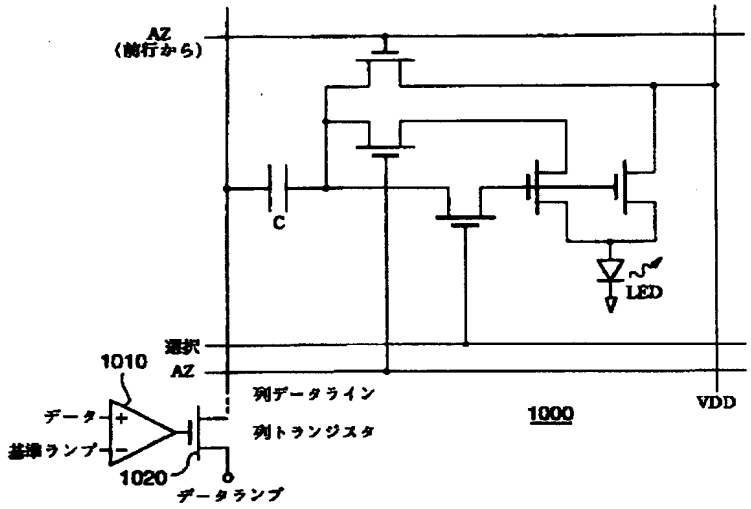
【図８】


プリチャージ
オートゼロ 書き込み
プリチャージ
(前行からの
オートゼロ)
データ
前行用データ
現在行用データ
オートゼロ
選択

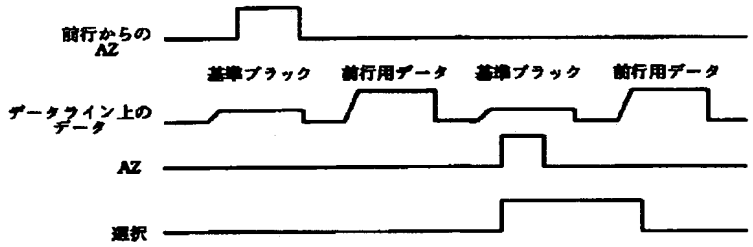
【図９】


プリチャージ
(前のオートゼロライン)
950
N5
N4
C
N1
N2
N3
LED
オートゼロ
選択
データ
900
992
VDD
VPRECHARGE

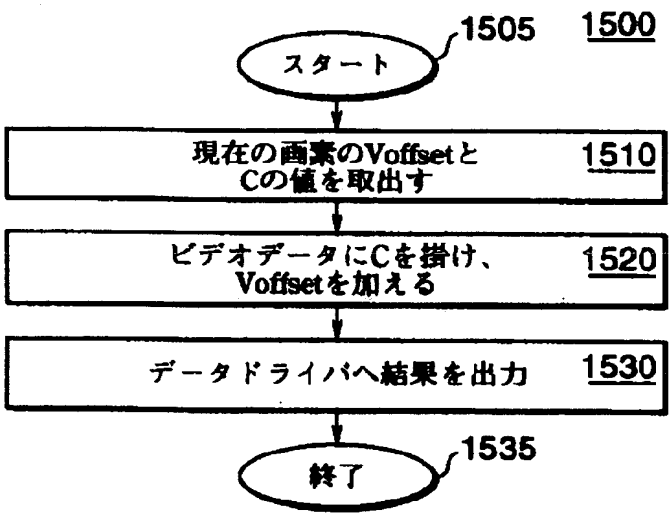
【図１０】


AZ
(前行から)
C
LED
選択
AZ
1010
データ
基準ランプ
列データライン
列トランジスタ
1000
VDD
1020
データランプ

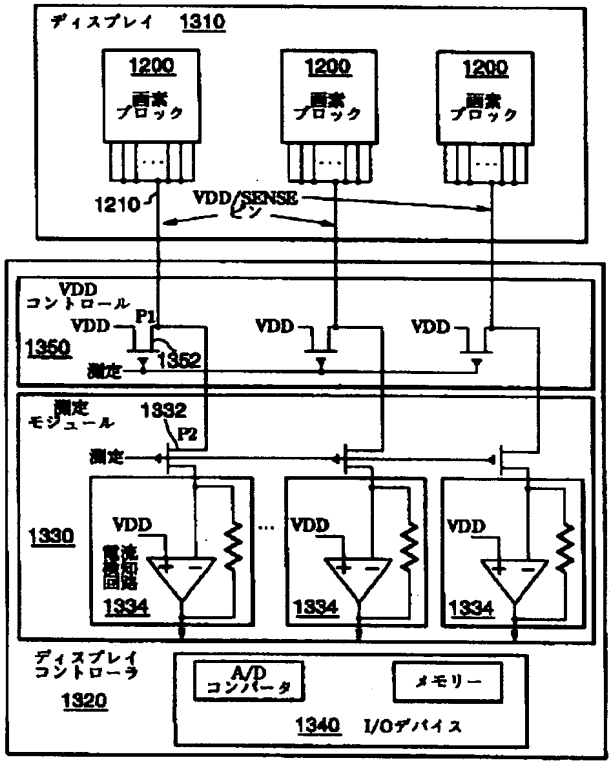
【図１１】


前行からの
AZ
基準ブラック
前行用データ
基準ブラック
前行用データ
データライン上の
データ
AZ
選択

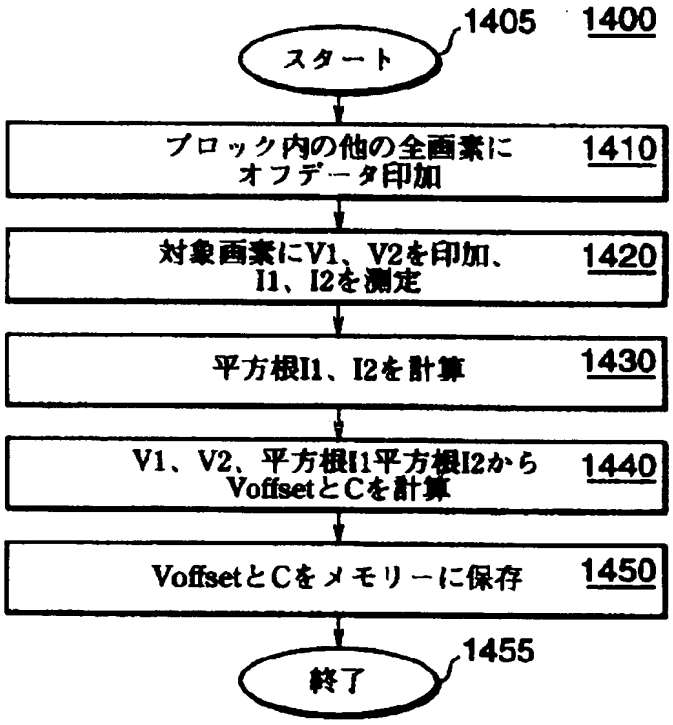
【図１５】


1505
1500
スタート
現在の画素のVoffsetと
Cの値を取出す
1510
ビデオデータにCを掛け、
Voffsetを加える
1520
データドライバへ結果を出力
1530
1535
終了

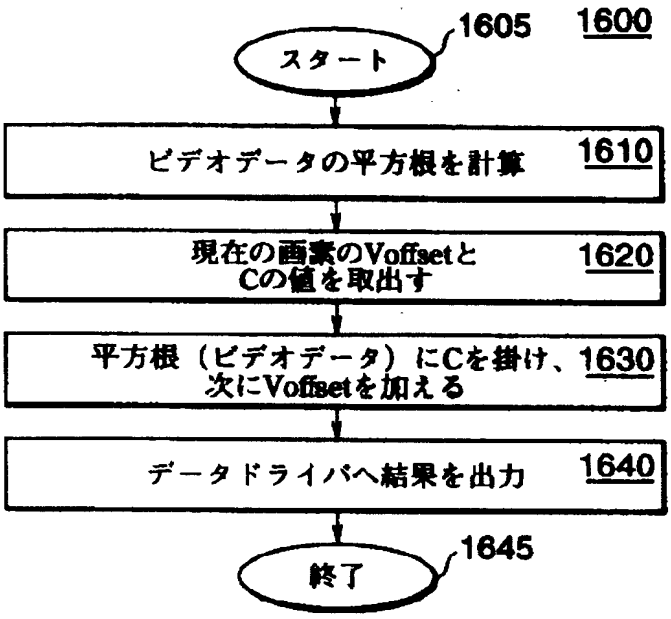
【図１３】


ディスプレイ 1310
1200
画素ブロック
1210
VDD/SENSE
VDD
コントロール
P1
1350
測定
1352
測定
モジュール
1332
P2
1330
1334
ディスプレイ
コントローラ
1320
A/D
コンバータ
メモリー
1340 I/Oデバイス

【図１４】


1405
1400
スタート
ブロック内の他の全画素に
オフデータ印加
1410
対象画素にV1、V2を印加、
I1、I2を測定
1420
平方根I1、I2を計算
1430
V1、V2、平方根I1平方根I2から
VoffsetとCを計算
1440
VoffsetとCをメモリーに保存
1450
1455
終了

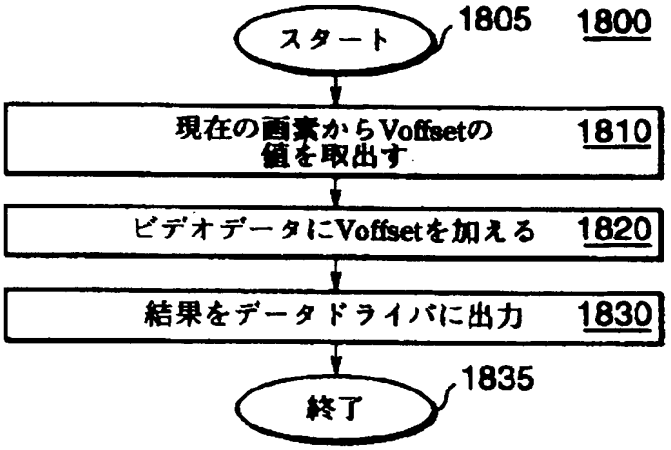
【図１６】


1605
1600
スタート
ビデオデータの平方根を計算
1610
現在の画素のVoffsetと
Cの値を取出す
1620
平方根（ビデオデータ）にCを掛け、
次にVoffsetを加える
1630
データドライバへ結果を出力
1640
1645
終了

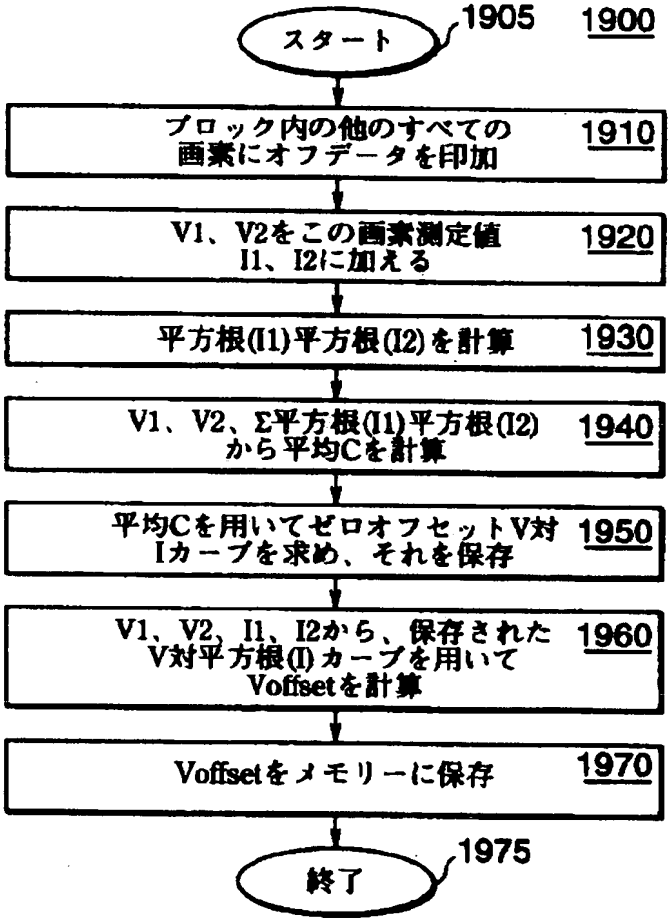
【図１７】


1705
1700
スタート
ブロック内の他のすべての
画素にオフデータを印加
1710
V1、V2を画素測定値
I1、I2に加える
1720
平方根(I1)平方根(I2)を計算
1730
V1、V2、Σ平方根(I1)平方根(I2)
から平均Cを計算
1740
V1、V2、平方根(I1)平方根(I2)、
CからVoffsetを計算
1750
Voffsetをメモリーに保存
1760
1765
終了

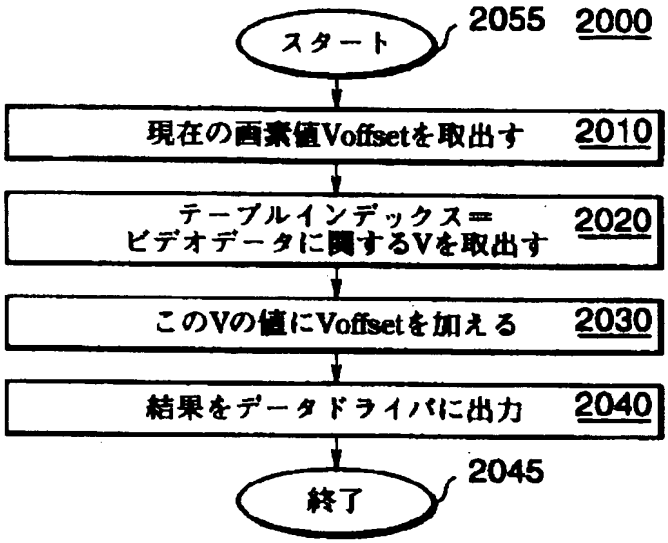
【図１８】


スタート
1805
1800
現在の画素からVoffsetの値を取出す
1810
ビデオデータにVoffsetを加える
1820
結果をデータドライバに出力
1830
終了
1835

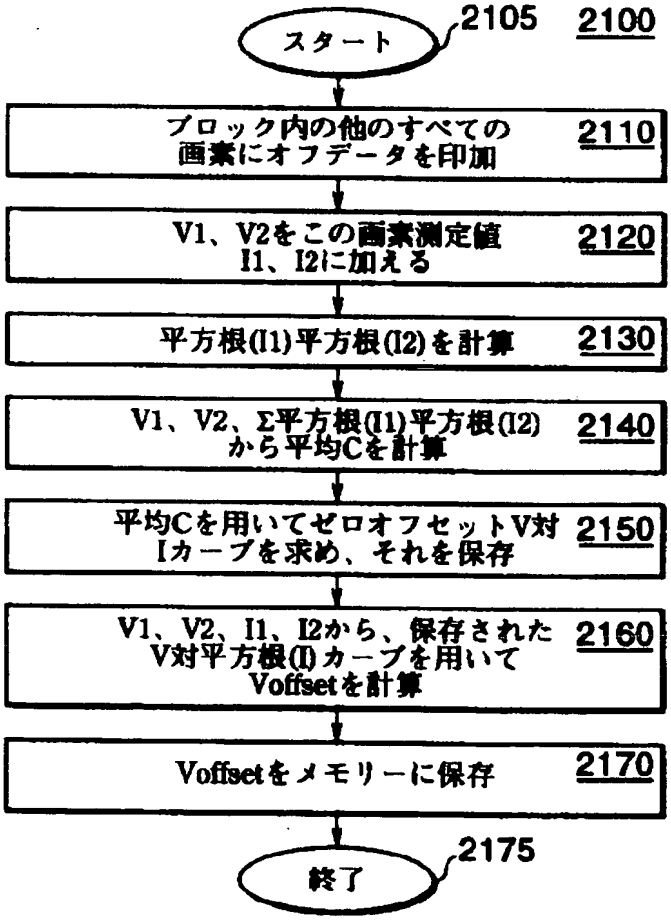
【図１９】


スタート
1905
1900
ブロック内の他のすべての画素にオフデータを印加
1910
V1、V2をこの画素測定値I1、I2に加える
1920
平方根(I1)平方根(I2)を計算
1930
V1、V2、Σ平方根(I1)平方根(I2)から平均Cを計算
1940
平均Cを用いてゼロオフセットV対Iカーブを求め、それを保存
1950
V1、V2、I1、I2から、保存されたV対平方根(I)カーブを用いてVoffsetを計算
1960
Voffsetをメモリーに保存
1970
終了
1975

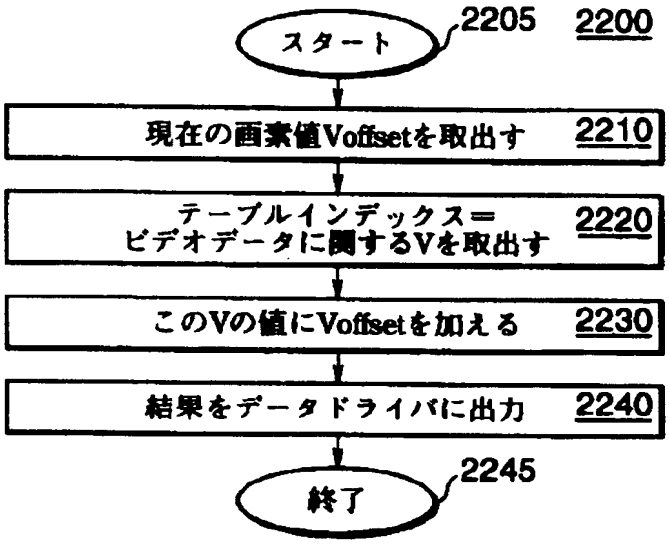
【図２０】


スタート
2055
2000
現在の画素値Voffsetを取出す
2010
テーブルインデックス＝
ビデオデータに関するVを取出す
2020
このVの値にVoffsetを加える
2030
結果をデータドライバに出力
2040
終了
2045

【図２１】


スタート
2105
2100
ブロック内の他のすべての
画素にオフデータを印加
2110
V1、V2をこの画素測定値
I1、I2に加える
2120
平方根(I1)平方根(I2)を計算
2130
V1、V2、Σ平方根(I1)平方根(I2)
から平均Cを計算
2140
平均Cを用いてゼロオフセットV対
Iカーブを求め、それを保存
2150
V1、V2、I1、I2から、保存された
V対平方根(I)カーブを用いて
Voffsetを計算
2160
Voffsetをメモリーに保存
2170
終了
2175

【図２２】



フロントページの続き

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【外国語明細書】

ACTIVE MATRIX LIGHT EMITTING DIODE PIXEL STRUCTURE AND CONCOMITANT METHOD

This application claims the benefit of U.S. Provisional Application No. 60/060, 386 filed September 29, 1997, and U.S. Provisional Application No. 60/060, 387 filed September 29, 1997, which are herein incorporated by reference.

The invention relates to an active matrix light emitting diode pixel structure. More particularly, the invention relates to a pixel structure that improves brightness uniformity by reducing current nonuniformities in a light-emitting diode of the pixel structure and method of operating said active matrix light emitting diode pixel structure.

BACKGROUND OF THE DISCLOSURE

Matrix displays are well known in the art, where pixels are illuminated using matrix addressing as illustrated in FIG. 1. A typical display 100 comprises a plurality of picture or display elements (pixels) 160 that are arranged in rows and columns. The display incorporates a column data generator 110 and a row select generator 120. In operation, each row is sequentially activated via row line 130, where the corresponding pixels are activated using the corresponding column lines 140. In a passive matrix display, each row of pixels is illuminated sequentially one by one, whereas in an active matrix display, each row of pixels is first loaded with data sequentially. Namely, each row in the passive matrix display is only "active" for a fraction of the total frame time, whereas each row in the active matrix display can be set to be "active" for the entire total frame time.

With the proliferation in the use of portable displays, e.g., in a laptop computer, various display technologies have been employed, e.g., liquid crystal display (LCD) and light-emitting diode (LED) display. Generally, an important criticality in portable displays is the ability to conserve power,

thereby extending the "on time" of a portable system that employs such display.

In a LCD, a backlight is on for the entire duration in which the display is in use. Namely, all pixels in a LCD are illuminated, where a "dark" pixel is achieved by causing a polarized layer to block the illumination through that pixel. In contrast, a LED display only illuminates those pixels that are activated, thereby conserving power by not having to illuminate dark pixels.

FIG. 2 illustrates a prior art active matrix LED pixel structure 200 having two NMOS transistors N1 and N2. In such pixel structure, the data (a voltage) is initially stored in the capacitor C by activating transistor N1 and then activating "drive transistor" N2 to illuminate the LED. Although a display that employs the pixel structure 200 can reduce power consumption, such pixel structure exhibits nonuniformity in intensity level arising from several sources.

First, it has been observed that the brightness of the LED is proportional to the current passing through the LED. With use, the threshold voltage of the "drive transistor" N2 may drift, thereby causing a change in the current passing through the LED. This varying current contributes to the nonuniformity in the intensity of the display.

Second, another contribution to the nonuniformity in intensity of the display can be found in the manufacturing of the "drive transistor" N2. In some cases, the "drive transistor" N2 is manufactured from a material that is difficult to ensure initial threshold voltage uniformity of the transistors such that variations exist from pixel to pixel.

Third, LED electrical parameters may also exhibit nonuniformity. For example, it is expected that OLED (organic light-emitting diode) turn-on voltages may increase under bias-temperature stress conditions.

Therefore, a need exists in the art for a pixel structure and concomitant method that reduces current nonuniformities due to threshold voltage variations in a "drive transistor" of the pixel structure.

SUMMARY OF THE INVENTION

The present invention incorporates a LED (or an OLED) pixel structure and method that improve brightness uniformity by reducing current nonuniformities in a light-emitting diode of the pixel structure. In one embodiment, a pixel structure having five transistors is disclosed. In an alternate embodiment, a pixel structure having three transistors and a diode is disclosed. In yet another alternate embodiment, a different pixel structure having five transistors is disclosed. In yet another alternate embodiment, an additional line is provided to extend the autozeroing voltage range. Finally, an external measuring module and various external measuring methods are disclosed to measure pixel parameters that are then used to adjust input pixel data.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a block diagram of a matrix addressing interface;

FIG. 2 depicts a schematic diagram of a prior art active matrix LED pixel structure;

FIG. 3 depicts a schematic diagram of an active matrix LED pixel structure of the present invention;

FIG. 4 depicts a timing diagram for active matrix LED pixel structure of FIG. 3;

FIG. 5 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure of the present invention;

FIG. 6 depicts a timing diagram for active matrix LED pixel structure of FIG. 5;

FIG. 7 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure of the present invention;

FIG. 8 depicts a timing diagram for active matrix LED pixel structure of FIG. 7;

FIG. 9 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure of the present invention;

FIG. 10 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure of the present invention;

FIG. 11 depicts a timing diagram for active matrix LED pixel structure of FIG. 10;

FIG. 12 illustrates a schematic diagram of an array of pixels interconnected into a pixel block;

FIG. 13 is a schematic diagram illustrating the interconnection between a display and a display controller;

FIG. 14 illustrates a flowchart of a method for initializing the display by measuring the parameters of all the pixels;

FIG. 15 illustrates a flowchart of a method for correcting input data representing pixel voltages;

FIG. 16 illustrates a flowchart of a method for correcting input video data representing pixel currents, i.e., luminances;

FIG. 17 illustrates a flowchart of a method for initializing the display by measuring the parameters of all the pixels where the video data represent pixel voltage;

FIG. 18 illustrates a flowchart of a method for correcting input video data representing pixel voltages;

FIG. 19 illustrates a flowchart of a method for initializing the display by measuring the parameters of all the pixels for the situation where the video data represents pixel currents;

FIG. 20 illustrates a flowchart of a method for correcting input video data represented in pixel currents, i.e., luminances;

FIG. 21 illustrates a flowchart of a method for initializing the display by measuring the parameters of all the pixels for the situation where the video data represents gamma-corrected luminance data;

FIG. 22 illustrates a flowchart of a method for correcting input video data represented in gamma-corrected luminance data; and

FIG. 23 depicts a block diagram of a system employing a display having a plurality of active matrix LED pixel structures of the present invention.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

FIG. 3 depicts a schematic diagram of an active matrix LED pixel structure 300 of the present invention. In the preferred embodiment, the active matrix LED pixel structure is implemented using thin film transistors (TFTs), e.g., transistors manufactured using poly-silicon or amorphous silicon. Similarly, in the preferred embodiment, the active matrix LED pixel structure incorporates an organic light-emitting diode (OLED). Although the present pixel structure is implemented using thin film transistors and an organic light-emitting diode, it should be understood that the present invention can be implemented using other types of transistors and light emitting diodes.

The present pixel structure 300 provides a uniform current drive in the presence of a large transistor threshold voltage (V_t) nonuniformity and OLED turn-on voltage nonuniformity. In other words, it is desirable to maintain a uniform current through the OLEDs, thereby ensuring uniformity in the intensity of the display.

Referring to FIG. 3, pixel structure 300 comprises five NMOS transistors N1 (310), N2 (320), N3 (330), N4 (340) and N5 (350), a capacitor 302 and a LED (OLED) (light element) 304 (light element). A Select line 370 is coupled to the gate of transistor 350. A Data line 360 is coupled to one terminal of the capacitor 302. An Autozero line 380 is coupled to the gate of transistor 340. A VDD line 390 is coupled to the drain of transistors 320 and 330. An Autozero line 382 from a previous row in the pixel array is coupled to the gate of transistor 330.

It should be noted that Autozero line 382 from a previous row can be implemented as a second Select line. Namely, the timing of the present pixel is such that the Autozero line 382 from a previous row can be exploited without the need of a second Select line, thereby reducing complexity and cost of the present pixel.

One terminal of the capacitor 302 is coupled (at node A) to the source of transistor 330 and to the drain of transistors 340 and 350. The source of

transistor 350 is coupled (at node B) to the gate of transistors 310 and 320. The drain of transistor 310 is coupled to the source of transistor 340. Finally, the source of transistors 310 and 320 are coupled to one terminal of the LED 304.

As discussed above, driving an organic LED display is challenging in light of the various nonuniformities. The present invention is an architecture for an organic LED display that addresses these criticalities. Namely, each LED pixel is driven in a manner that is insensitive to variations in the LED turn-on voltage, as well as to variations in the TFT threshold voltages. Namely, the present pixel is able to determine an offset voltage parameter using an autozeroing method that is used to account for these variations in the LED turn-on voltage, and the TFT threshold voltages.

Furthermore, data is provided to each pixel as a data voltage in a manner that is very similar to that used in conventional active-matrix liquid crystal displays. As a result, the present display architecture can be employed with conventional column and row scanners, either external or integrated on the display plate.

The present pixel uses five (5) TFTs and one capacitor, and the LED. It should be noted that TFTs are connected to the anode of the LED, and not the cathode, which is required by the fact that ITO is the hole emitter in conventional organic LED. Thus, the LED is coupled to the source of a TFT, and not the drain. Each display column has 2 row lines (the auto-zero line and the select line), and 1 1/2 column lines (the data line and the +Vdd line, which is shared by neighboring columns). The waveforms on each line are also shown in FIG. 4. The operation of the pixel 300 is described below in three phases or stages.

The first phase is a precharge phase. A positive pulse on the auto-zero (AZ) line of the previous row 382 turns "on" transistor 330 and precharges node A of the pixel up to Vdd, e.g., +10 volts. Then the Data line changes from its baseline value to write data into the pixel of the previous

row, and returns to its baseline. This has no net effect on the pixel under consideration.

The second phase is an auto-zero phase. The AZ and SELECT lines for the present row go high, turning "on" transistors 340 and 350 and causing the gate of transistor N1 310 to drop, self-biasing to a turn-on voltage that permits a very small trickle of current to flow through the LED. In this phase the sum of the turn-on voltage of the LED and the threshold voltage of N1 are stored on the gate of N1. Since N1 and N2 can be placed very close together, their initial threshold voltages will be very similar. In addition, these two transistors should have the same gate to source voltage, Vgs. Since a TFT threshold drift depends only on Vgs over the life of the TFT, it can be assumed that the threshold voltages of these devices will track over the life of the TFT. Therefore, the threshold voltage of N2 is also stored on its gate. After auto-zeroing is complete, the Autozero line returns low, while Select line stays high.

The third phase is a data writing phase. The data is applied as a voltage above the baseline voltage on the Data line, and is written into the pixel through the capacitor. Then, the Select line returns low, and the sum of the data voltage, plus the LED turn-on voltage, plus N2's threshold voltage, is stored at node B for the rest of the frame. It should be noted that a capacitor from node B to +Vdd can be employed in order to protect the stored voltage from leaking away.

In sum, during the auto-zero phase, the LED's turn-on voltage, as well as N2's threshold voltage, are "measured" and stored at node B using a trickle current. This auto-zero phase is essentially a current-drive mode of operation, where the drive current is very small. It is only after the auto-zero phase, in the writing phase, that the voltage on the LED is incremented above turn-on using the applied data voltage. Thus, the present invention can be referred to as having a "hybrid drive," rather than a voltage drive or current drive. The hybrid drive method combines the advantages of voltage drive and current drive, without the disadvantages of either. Variations in the turn-on voltage of the LED and the threshold

voltage of the TFT are corrected, just as in current drive. At the same time, all lines on the display are driven by voltages, and can therefore be driven fast.

It should be noted that the data voltage increment applied to the Data line 360 does not appear directly across the LED 304, but is split between Vgs of N2 320 and the LED. This simply means that there is a nonlinear mapping from the data voltage to the LED voltage. This mapping, combined with the nonlinear mapping from LED voltage to LED current, yields the overall transfer function from data voltage to LED current, which is monotonic, and, as noted above, is stable over the life of the display.

An advantage of the present pixel architecture 300 is that the transistors in the pixel whose threshold shifts are uncorrected (N3, N4, and N5) are turned on for only one row-time per frame, and therefore have a very low duty-cycle and are not expected to shift appreciably. Additionally, N2 is the only transistor in the LED's current path. Additional transistors connected in series on this path may degrade display efficiency or may create problems due to uncorrected TFT threshold shifts, and, if shared by all pixels on a column, may introduce significant vertical crosstalk.

Select and Autozero (AZ) pulses are generated by row scanners. The column data is applied on top of a fixed (and arbitrary) baseline voltage in the time-slot between AZ pulses. The falling edge of Select signal occurs while data is valid on the Data line. Various external and integrated column-scanner designs, either of the direct-sample or chopped-ramp type, can produce data with this timing.

The above pixel architecture permits large direct-view displays to be built using organic LEDs. Of course, the present pixel structure is also applicable to any display technology that uses display elements requiring drive current, particularly, when the display elements or the TFTs have turn-on voltages that shift or are nonuniform.

FIG. 5 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure 500 of the present invention. The pixel

structure 500 is similar to the pixel structure 300 of FIG. 3, where a Schottky diode is now employed in lieu in of two transistors.

One potential disadvantage of the pixel structure 300 is the use of five transistors per pixel. Namely, using so many transistors in each pixel may impact the pixel's fill-factor (assuming bottom-side emission through the active plate), and also its yield. As such, the pixel structure 300 employs a single Schottky diode in each pixel that reduces the number of transistors from five to three transistors, while performing the same functions as previously described.

Referring to FIG. 5, pixel structure 500 comprises three NMOS transistors N1 (510), N2 (520), N3 (530), a capacitor 502, a Schottky diode 540 and a LED (OLED) 550 (light element). A Select line 570 is coupled to the gate of transistor 530. A Data line 560 is coupled to one terminal of the capacitor 502. An Autozero line 580 is coupled to the gate of transistor 520. An Illuminate (similar to a VDD line) line 590 is coupled to one terminal of the Schottky diode 540.

One terminal of the capacitor 502 is coupled (at node A) to the drain of transistors 520 and 530. The source of transistor 530 is coupled (at node B) to the gate of transistor 510. The drain of transistor 510 is coupled to the source of transistor 520, and one terminal of the Schottky diode 540.

The pixel structure 500 also has three phases of operation: a precharge phase, an autozero phase, and a data writing phase as discussed below. All of the Illuminate lines are connected together at the periphery of the display, and before the precharge phase begins, the Illuminate lines are held at a positive voltage V_{ILL}, which is approximately +15V. For the purpose of the following discussion, a row under consideration is referred to as "row i". The waveforms on each line are also shown in FIG. 6.

The first phase is a precharge phase. Precharge is initiated when the Autozero (AZ) line turns on transistor N2, and the Select line turns on transistor N3. This phase is performed while the Data line is at a reset level. The voltage at Nodes A and B rises to the same voltage as the drain of transistor N1, which is a diode drop below V_{ILL}.

The second phase is an autozero phase. Next, the Illuminate line drops to ground. During this phase, all pixels on the array will briefly darken. Autozeroing of N1 now begins with the Schottky diode 540 causing the drain of transistor N1 to be isolated from the grounded Illuminate line. When Node B has reached a voltage approximately equal to the threshold voltage of the transistor N1 plus the turn-on voltage of the LED 550, the AZ line is used to turn transistor N2 "off", and the Illuminate line is restored to V_{ILL}. All pixels in unselected rows light up again.

The third phase is a data writing phase. Next, the data for row i is loaded onto the data line. The voltage rise at Nodes A and B will equal the difference between the Data line's reset voltage level and the data voltage level. Thus, variations in the threshold voltage of transistor N1 and the LED's turn-on voltage will be compensated. After the voltage at Node B has settled, the Select line for row i is used to turn off transistor N3, and the Data line is reset. The proper data voltage is now stored on the pixel until the next frame.

Thus, a three-transistor pixel for OLED displays has been described, that possesses the advantages described previously for the 5-transistor pixel 300, but requires fewer transistors. An additional advantage is that the 5-transistor pixel employs separate transistors for autozeroing and driving the LED. Proper operation of pixel 300 requires that these two transistors have matching initial thresholds that would drift over life in the same way. Recent experimental data suggest that TFTs with different drain voltages (as these two transistors have) may not drift in the same way. Thus, pixel 500 performs autozeroing on the same transistor that drives the LED, such that proper autozeroing is guaranteed.

FIG. 7 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure 700 of the present invention. The pixel structure 700 is similar to the pixel structure 300 of FIG. 3, with the exception that pixel structure 700 may generate a more precise autozero voltage.

Namely, referring to FIG. 3, the autozeroing arises from the fact that each precharge cycle, as shown in FIG. 3, injects a large positive charge Q_{PC} onto Node A of the pixel 300. During the precharge phase, nearly all of the capacitance on Node A is from capacitor C_{data}, such that the charge injected onto Node A is:

$$Q_{PC} \equiv C_{data}(V_{DD} - V_A) \tag{1}$$

where V_A is the voltage that was on Node A before the precharge phase began. V_A depends on the threshold voltage of N3 330 and the turn-on voltage of the LED 304, as well as the previous data applied to the pixel 300. Since C_{data} is a large capacitance (approx. 1 pF), Q_{PC} is also relatively large, on the order of ten picocoulombs.

When the pixel 300 is at a stable autozero level, Q_{PC} flows through N1 310 and the LED 304 during the autozero phase. Since the autozero interval is short (approximately 10 μsec.), N1 may be left with a gate-to-source autozero voltage higher than its threshold voltage, and similarly the LED autozeroes above its turn-on voltage. Thus, the autozeroing process may not produce a true zero-current autozero voltage at Nodes A and B, but instead, an approximation of a zero-current autozero voltage.

It should be noted that it is not necessary to produce a true zero-current autozero voltage, corresponding to exactly zero current through N1 and the LED. The desirable goal is to obtain an autozero voltage that permits a small trickle of current (approximately ten nanoamps) to flow through N1 310 and the LED 304. Since the autozero interval is approximately 10 μsec, then Q_{PC} should be on the order of 0.1 picocoulomb. As noted above, Q_{PC} is approximately 10 picocoulombs.

The effect of such a large Q_{PC} is that the pixel's stable autozero voltage may well be above the sum of the threshold and turn-on voltages. This condition by itself is not a problem, if the excess autozero voltages were

uniform across the display. Namely, the effect can be addressed by offsetting all the data voltages accordingly.

However, a potential difficulty may arise if Q_{PC} is not only large, but also depends on the previous data voltage, and on the autozero voltage itself. If this condition develops in the display, then not only will all pixels have large excess autozero voltages, but also the magnitude of the excess voltage may vary from pixel to pixel. In effect, the autozeroing of pixel 300 may not produce a uniform display under such a condition.

To address this criticality, the pixel structure 700 is capable of reducing the precharge Q_{PC} to a very small value. Additionally, a "variable precharge" method is disclosed, that permits Q_{PC} to vary, depending on the amount of charge that is actually needed for autozeroing. In brief, if the current autozero voltage is too low, Q_{PC} assumes its maximum value of about 0.1 picocoulomb in order to raise the autozero voltage toward its desired value. However, if the current autozero voltage is too high, then Q_{PC} is essentially zero, allowing the autozero voltage to drop quickly.

Referring to FIG. 7, pixel structure 700 comprises five NMOS transistors N1 (710), N2 (720), N3 (730) , N4 (740), N5 (750), a capacitor 702, and a LED (OLED) 704 (light element). A Select line 770 is coupled to the gate of transistor 710. A Data line 760 is coupled to one terminal of the capacitor 702. An Autozero line 780 is coupled to the gate of transistor 740. A VDD line 790 is coupled to the drain of transistors 720 and 750. An Autozero line 782 from a previous row in the pixel array is coupled to the gate of transistor 750.

It should be noted that Autozero line 782 from a previous row can be implemented as a second Select line. Namely, the timing of the present pixel is such that the Autozero line 782 from a previous row can be exploited without the need of a second Select line, thereby reducing complexity and cost of the present pixel.

One terminal of the capacitor 702 is coupled (at node A) to the drain of transistor 710. The source of transistor 710 is coupled (at node B) to the gate of transistors 720 and 730 and is coupled to the source of transistor

740. The drain of transistor 740 is coupled (at node C) to the source of transistor 750, and to the drain of transistor 730. Finally, the source of transistors 730 and 720 are coupled to one terminal of the LED 704.

More specifically, the pixel 700 is similar to the pixel 300, except that the precharge voltage is now applied to Node C, which is the drain of transistor N3 730. In addition, there are also some timing changes as shown in FIG. 8. The operation of the pixel 700 is again described below in three phases or stages.

The first phase is a precharge phase that occurs during the previous line time, i.e., before data is applied to the previous row's pixels. A positive pulse on the Select line turns "on" N1, thereby shorting Nodes A and B together, which returns the pixel 700 to the state it was in after the last autozero phase. Namely, the pixel is returned to a data-independent voltage that is the pixel's most recent estimate of its proper autozero voltage. While transistor N1 is "on", a positive pulse on the Autozero line 782 from a previous row line turns "on" transistor N5, thereby precharging Node C to V_{dd}. In turn, transistors N1 and N5 are turned "off".

The relative timing of turning transistors N1 and N5 "on" and "off" is not very important, except that transistor n1 must be "on" before transistor N5 is turned "off". Otherwise, transistor N3 may still be turned "on" in response to the old data voltage, and the charge injected onto Node C may inadvertently drain away through transistor N3.

After the precharge phase, the charge Q_{PC} is stored at Node C on the gate-to-source/drain capacitances of transistors N3, N4 and N5. Since these capacitances add up to a very small capacitance (about 10 fF), and the precharge interval raises Node C about 10V, Q_{PC} is initially approximately 0.1 picocoulombs. However, this charge will drain from Node C to varying degrees prior to the autozero phase, depending on how well the previous autozero voltage approximates the true autozero voltage. Thus, it is more accurate to indicate that $Q_{PC} \leq 0.1$ picocoulomb, depending on how much charge is needed for autozeroing. This is the variable precharge feature. If the last autozero voltage is too low, N3 is nonconducting after the precharge

phase, and Q_{PC} should stay at its maximum value, raising the autozero voltage toward its desired level during the autozero phase. If the last autozero voltage is too high, N3 is conducting, and Q_{PC} will drain off by the time the autozero phase occurs, allowing the autozero voltage to drop quickly.

Although the relative timing for transistors N1 and N5 is not critical, the preferred timing is shown in FIG. 8. The two transistors N1 and N5 turn "on" at the same time in order to minimize the time required for precharge. N1 turns "off" before N5 such that the (intentional) draining of Q_{PC} from Node C is in response to a Node B voltage that has been capacitively pushed down by N1 turning "off". This ensures that the draining of Q_{PC} from Node C is in response to a Node B voltage that is the same as when zero data is applied to the pixel.

In sum, the pixel 700 when compared to the pixel 300, provides a means of precharging the pixel that allows a more effective autozeroing. Specifically, the autozeroing of pixel 700 is more accurate, faster, and data independent. Computer simulations have verified that the pixel 700 autozeroes well and is able to maintain a nearly constant OLED current vs. data voltage characteristic over an operational lifetime of 10,000 hours.

FIG. 9 depicts a schematic diagram of an alternate embodiment of an active matrix LED pixel structure 900 of the present invention. The pixel structure 900 is similar to the pixel structure 700 of FIG. 7, with the exception of having an additional $V_{precharge}$ line 992, that permits the range of autozero voltages to be extended without raising the LED supply voltage V_{dd}. This additional modification of the pixel extends the life and efficiency of the pixel.

It should be noted that the above described pixels (200, 300, 700) have the limitation that the autozero voltage cannot exceed V_{dd}, since this is the precharge voltage. However, as the threshold voltages of transistors N2 and N3 drift over the life of the transistor, a point is reached where an autozero voltage higher than V_{dd} is required in order to compensate for drift in the TFT threshold voltage and in the OLED turn-on voltage. Since the

autozero voltage cannot reach higher voltages, display uniformity will quickly degrade, signaling the end of the useful life of the display. Raising V_{dd} will permit higher autozero voltages to be achieved, but at the expense of power efficiency, since V_{dd} is also the OLED drive supply.

Furthermore, the range of autozero voltages will be restricted even further if, in order to improve power efficiency, V_{dd} is reduced to operate transistor N2 in the linear region. (Of course, this will require N2 to be made larger than if it was operated in saturation.) In this case, the operating lifetime will be quite short, since after a short period of operation, the autozero voltage will need to reach a level higher than V_{dd}.

Referring to FIG. 9, an optional modification is incorporated into the pixel 700 that removes restrictions on the autozero voltage, thereby permitting it to be extended to well above V_{dd}. The pixel 900 is identical to the pixel 700 with the exception of an additional column line 992, that is coupled to the drain of transistor 950.

The column line 992 is added to the array to carry a DC voltage $V_{precharge}$ to all the pixels. All of these column lines are connected together at the edge of the display. By raising $V_{precharge}$ to a level higher than V_{dd}, the pixel 900 can precharge and autozero to a voltage higher than V_{dd}. A high value of $V_{precharge}$ will have very little effect on display efficiency.

It should be noted that each $V_{precharge}$ line 992 can be shared by neighboring columns of pixels. The $V_{precharge}$ lines can also run as row lines, shared by neighboring rows.

In sum, a modification of the above OLED pixels is disclosed where an additional voltage line is provided to extend the range of the autozero voltages beyond V_{dd}. This allows the OLED drive transistor to operate at as low a voltage as needed for power efficiency, possibly even in the linear region, without restricting the range of autozero voltages. Thus, long operating lifetime and high efficiency can be obtained. Finally, although the present modification is described with respect to pixel 700, it should be understood that this optional modification can be employed with other

autozeroing pixel structures, including but not limited to, pixels 200 and 300 as discussed above.

Although the above pixel structures are designed for an OLED display in such a manner that transistor threshold voltage variations and OLED turn-on voltage variations in the pixel can be compensated, these pixel structures are not designed to address nonuniformity that is generated external to the pixel. It was pointed out that the pixel could be used with conventional column driver circuits, either external to the display plate or integrated on the display.

Unfortunately, integrated data drivers are typically not as accurate as external drivers. While commercially available external drivers can achieve ±12 mV accuracy, it has proven difficult to achieve accuracy better than ±50 mV using integrated drivers. The particular type of error produced by integrated drivers is primarily offset error, i.e., it is a data-independent DC level that adds to all data voltages. The offset error is nonuniform, i.e., the value of the DC level varies from one data driver to the next. Liquid crystal displays tend to be forgiving of offset errors because the liquid crystal is driven with opposite polarity data in successive frames, such that in one frame the offset error causes the liquid crystal to be slightly too dark, and in the next frame too light, but the average is nearly correct and the alternating errors are not noticeable to the eye. However, an OLED pixel is driven with unipolar data. Therefore, the bipolar cancellation of offset errors does not occur, and serious nonuniformity problems may result when integrated scanners are used.

FIG. 10 depicts a schematic diagram of an active matrix LED pixel structure 300 of the present invention coupled to a data driver 1010 via a column transistor 1020. The present invention describes a method for canceling offset errors in integrated data scanners for OLED displays. Namely, the present method is designed to operate with any pixel in which the pixel is capacitively coupled to a data line, and has an autozero phase, e.g., pixels 200, 300, 500, and 700 as discussed above.

Referring to FIG. 10, the pixel 300 as described above is coupled to a Data line that provides the pixel with an analog level to establish the brightness of the OLED element. In FIG. 10, the Data line is driven by a data driver that uses the chopped ramp technique to set the voltage on the Data line. Various sources of error exist in this approach that may give rise to offset errors on the Data line. For example, the time at which the voltage comparator switches can vary depending on the comparator's maximum slew rate. It has also been observed experimentally that the maximum slew rate can be highly variable. The offset error will affect the voltage stored in the pixel. Since it is nonuniform, the offset error will also lead to brightness variations across the display.

In the present invention, the period during which the pixel autozeros to cancel its own internal threshold error is also used to calibrate out the data scanner's offset error. The waveforms of the various lines is shown in FIG. 11.

Namely, this is accomplished by setting a reference black level on the Data line using the same column driver that will apply the actual data voltage. This reference black level, applied during the pixel's autozero phase, is set on the Data line in exactly the same manner that the actual data voltage will be set: the data ramp is chopped at a time determined by the voltage comparator. Thus, the voltage across capacitor C of the pixel is determined by the difference between the pixel's turn-on voltage and the combined black level plus the offset error voltage. The reference black level is maintained for the entire autozero phase. When the actual data is applied to the pixel, the data scanner offset error is now canceled by the stored voltage on the pixel capacitor.

This technique can be applied not only to integrated scanners that use a chopped ramp, but also to scanners using direct sampling onto the columns. In the case of direct sampling, the error arises from the nonuniform capacitive feedthrough of the gate signal onto the Data line when the (large) column transistor turns off. Variations in the threshold voltage of this transistor produce a nonuniform offset error, just like the

nonuniform offset error produced by the chopped ramp data scanners.

Thus, it can be corrected in the same manner. A black reference voltage is written onto the columns during the pixel's autozero phase. Since all of the pixels in a row autozero at the same time, this black level is written onto all of the data columns simultaneously at the beginning of the line time. The black level is maintained for the entire autozero phase. As in the case of the chopped-ramp scanner, when the actual data is applied to the pixel, the offset error will be canceled by the voltage stored on the pixel capacitor. However, it seems likely that the time overhead required to perform offset error correction is smaller using the direct-sampling technique than with the chopped ramp technique.

The present method for correcting data driver errors should permit organic LED displays to be built with much better brightness uniformity than would otherwise be possible. Using the method described here, together with any of the above autozeroing pixels, brightness uniformity of 8-bits should be achievable, with no visible uniformity degradation over the lifetime of the display.

Although the above disclosure describes a plurality of pixel structures that can be employed to account for nonuniformity in the intensity of a display, an alternative approach is to compensate such nonuniformity by using external means. More specifically, the disclosure below describes an external calibration circuit and method to account for nonuniformity in the intensity of a display. In brief, the non-uniformity is measured and stored for all the pixels such that the data (e.g., data voltages) can be calibrated using the measured non-uniformity.

As such, although the conventional pixel structure of FIG. 2 is used in the following discussion, it should be understood that the present external calibration circuit and method can be employed with other pixel structures, including but not limited to, the pixels 300, 500, and 700 as described above. However, if the non-uniformity is addressed by the present external calibration circuit and method, then a more simplified pixel structure can be employed in the display, thereby increasing display yield and fill-factor.

FIG. 12 illustrates a schematic diagram of an array of pixels 200 interconnected into a pixel block 1200. Referring to FIG. 2, in operation, data is written into the pixel array in the manner commonly used with active matrix displays. Namely, a row of pixels is selected by driving the Select line high, thereby turning on access transistor N1. Data is written into the pixels in this row by applying data voltages to the Data lines. After the voltage at node A has settled, the row is deselected by driving the Select line low. The data voltage is stored at node A until this row is selected again on the next frame. There may be some charge leakage from node A during the time that N1 is turned off, and a storage capacitor may be required at node A to prevent an unacceptable level of voltage decay. The dotted lines illustrate how a capacitor can be connected to address the voltage decay. However, it is possible that there is sufficient capacitance associated with the gate of N2 to render such additional capacitance unnecessary.

It should be noted that the luminance L of an OLED is approximately proportional to its current I, with the constant of proportionality being fairly stable and uniform across the display. Therefore, the display will be visually uniform if well-defined OLED currents are produced.

However, what is programmed into the pixel is not the OLED current, but rather the gate voltage on N2. It is expected that TFT threshold voltages and transconductances will exhibit some initial nonuniformity across a display, as will the OLED electrical parameters. Furthermore, it is well known that TFT threshold voltages increase under bias-temperature stress conditions, as do OLED turn-on voltages. Thus, these parameters are expected to be initially nonuniform, and to vary over the life of the pixel in a manner that depends on the individual bias history of each pixel. Programming the gate voltage of N2 without compensating for the variations of these parameters will yield a display that is initially nonuniform, with increasing nonuniformity over the life of the display.

The present invention describes a method for correcting the data voltage applied to the gate of N2 in such a way that variations in the TFT

and OLED electrical parameters are compensated, thereby permitting well-defined OLED currents to be produced in the pixel array.

FIGs. 2 and 12 illustrate a pixel array having VDD supply lines that are disposed parallel to the Data lines. (In alternative embodiments, the VDD lines may run parallel to the Select lines.) As such, each VDD line can be shared by two or more neighboring columns of pixels to reduce the number of VDD lines. Figure 12 illustrates the VDD lines as being tied together into blocks on the periphery of the display. Each pixel block 1200 may contain as few as one VDD line, or as many as the total number of VDD lines on the display. However, in the preferred embodiment, each pixel block 1200 contain about 24 VDD lines, i.e., about 48 pixel columns.

FIG. 13 is a schematic diagram illustrating the interconnection between a display 1310 and a display controller 1320. The display 1310 comprises a plurality of pixel blocks 1200. The display controller 1320 comprises a VDD control module 1350, a measurement module 1330 and various I/O devices 1340 such as A/D converters and a memory for storing pixel parameters.

Each pixel block is coupled to a sensing pin (VDD/SENSE) 1210 at the edge of the display, as shown in FIGs. 12 and 13. During normal display operation, the sensing pins 1210 are switched to an external V_{dd} supply, e.g., between 10-15V, thereby supplying current to the display for illuminating the OLED elements. More specifically, each VDD/SENSE pin 1210 is associated with a pair of p-channel transistors P1 (1352) and P2 (1332) and a current sensing circuit 1334 in the display controller 1320. During normal operation, an ILLUMINATE signal from the display controller activates P1 to connect a VDD/SENSE pin to the V_{dd} supply. In a typical implementation, the current through P1 is expected to be approximately 1 mA per column.

In order to compensate for variations in the TFT and OLED parameters, the external current sensing circuits 1334 are activated via a MEASURE signal to collect information about each pixel's parameters during a special measurement cycle. The collected information is used to

calculate or adjust the appropriate data voltages for establishing the desired OLED currents during normal display operation.

More specifically, during a given pixel's measurement cycle, all other pixels in the pixel block are tuned off by loading these pixels with low data voltages (e.g., zero volts or less), thereby ensuring negligible current draw from the "off" pixels. In turn, the current drawn by the pixel of interest is measured in response to one or more applied data voltages. During each measurement cycle, the data pattern (i.e., consisting of all pixels in a block turned "off" except for one pixel turned "on") is loaded into the pixels in the normal way, with data applied to the DATA lines by data driver circuits, and rows being selected one by one. Thus, since the display is partitioned into a plurality of pixel blocks, a plurality of pixels can be measured by turning on at least one pixel in each pixel block simultaneously.

The current drawn by the pixel of interest in each pixel block is measured externally by driving the ILLUMINATE and MEASURE lines to levels that disconnect the VDD/SENSE pin 1210 from VDD source and connect the sensing pin to the input of a current-sensing circuit 1334 through P2, where the current drawn by the pixel of interest is measured. The pixel current is expected to be in the range of 1-10 uA. The current-sensing circuit 1334 is shown as a transimpedance amplifier in FIG. 13, but other embodiments of current-sensing circuit can be implemented. In the present invention, the amplifier generates a voltage at the output that is proportional to the current at the input. This measured information is then collected by I/O devices 1340 where the information is converted into digital form and then stored for calibrating data voltages. The resistor in the current-sensing circuit 1334 is approximately one Megohm.

Although multiple current-sensing circuits 1334 are illustrated with a one to one correspondence with the pixel blocks, fewer current-sensing circuits can be employed through the use of a multiplexer (not shown). Namely, multiple VDD/SENSE pins are multiplexed to a single current-sensing circuit 1334. In one extreme, a single current-sensing circuit is used for the entire display. Multiplexing the VDD/SENSE pins to the

sensing circuits in this manner reduces the complexity of the external circuitry, but at the expense of added display measurement time.

Since normal display operation must be interrupted in order to perform pixel measurement cycles, pixel measurements should be scheduled in a manner that will least disrupt the viewer. Since the pixel parameters change slowly, a given pixel does not need to be measured frequently, and measurement cycles can be spread over a long period of time.

While it is not necessary for all pixels to be measured at the same time, it is advantageous to do so in order to avoid nonuniformity due to variable measurement lag. This can be accomplished by measuring all pixels rapidly when the display module is turned "on", or when it is turned "off". Measuring pixels when the display module is turned "off" does not interfere with normal operation, but may have the disadvantage that after a long "off" period, the stored pixel parameters may no longer ensure uniformity. However, if an uninterrupted power source is available (e.g., in screen saver mode), measurement cycles can be performed periodically while the display is "off" (from the user's point of view). Of course, any option that does not include a rapid measurement of all pixels when the display module is turned "on", requires that nonvolatile memory be available for storing measurement information while power is "off".

If pixel measurement information is available, compensation or calibration of the data voltages can be applied to the display to correct for various sources of display nonuniformity. For example, compensation of the data voltages can be performed to account for transistor threshold-voltage variations and OLED turn-on voltage variations. As such, the discussion below describes a plurality of methods that are capable of compensating the above sources of display nonuniformity, including other sources of display nonuniformity as well. By using these methods, a display with several sources of nonuniformity, some of them severe, can still provide a uniform, high-quality displayed image.

For the purpose of describing the present compensation methods, it is assumed that the pixel structure of FIG. 2 is employed in a display.

However, it should be understood that the present compensation methods can be adapted to a display employing any other pixel structures.

Referring to FIG. 2, the stored voltage on Node A is the gate voltage of N2, and thus establishes a current through N2 and through the LED. By varying the gate voltage on N2, the LED current can be varied. Consider the relationship between the gate voltage on N2 and the current through the LED. The gate voltage V_g can be divided into two parts, the gate-to-source voltage V_{gs} of N2 and the voltage V_{diode} across the LED:

$$V_g = V_{gs} + V_{diode} \tag{2}$$

For an MOS transistor in saturation the drain current is approximately:

$$I = \frac{k}{2}(V_{gs} - V_t)^2 \tag{3}$$

where k is the device transconductance parameter and V_t is the threshold voltage. (For operation in the linear region, see below.) Therefore:

$$V_{gs} = \sqrt{\frac{2I}{k}} + V_t \tag{4}$$

The forward current through the OLED is approximately:

$$I = AV_{diode}^m \tag{5}$$

where A and m are constants (See Burrows et al., J. Appl. Phys. 79 (1996)). Therefore:

$$V_{diode} = \sqrt[m]{\frac{I}{A}} \tag{6}$$

Thus, the overall relation between the gate voltage and the diode current is:

$$V_g = V_t + \sqrt{\frac{2I}{k}} + \sqrt{\frac{I}{A}} \qquad (7)$$

It should be noted that other functional forms can be used to represent the OLED I-V characteristic, which may lead to different functional relationships between the gate voltage and the diode current. However, the present invention is not limited to the detailed functional form of the OLED I-V characteristic as disclosed above, and as such, can be adapted to operate for any diode-like characteristic.

The luminance L of an OLED is approximately proportional to its current I, with the constant of proportionality being fairly stable and uniform across the display. Typically, the display is visually uniform if well-defined OLED currents can be produced. However, as discussed above, the pixel is programmed with the voltage V_g and not the current I. The problem is based on the observation that TFT parameters V_t and k will exhibit some initial nonuniformity across a display, as well OLED parameters A and m. Furthermore, it is well known that V_t increases under bias-temperature stress conditions. The OLED parameter A is directly related to the OLED's turn-on voltage, and is known to decrease under bias stress. The OLED parameter m is related to the distribution of traps in the organic band gap, and may also vary over the life of the OLED. Thus, these parameters are expected to be initially nonuniform, and to vary over the life of the display in a manner that depends on the individual bias history of each pixel. Programming the gate voltage without compensating for the variations of these parameters will yield a display that is initially nonuniform, with increasing nonuniformity over the life of the display.

In fact, other sources of nonuniformity exists. The gate voltage V_g is not necessarily equal to the intended data voltage V_{data}. Instead, gain and offset errors in the data drivers, as well as (data-dependent) feedthrough arising from the deselection of N1, may cause these two voltages to be different. These sources of error can also be nonuniform and can vary over

the life of the display. These and any other gain and offset errors can be addressed by expressing:

$$V_g = BV_{data} + V_0 \tag{8}$$

where B and V_0 are a gain factor and an offset voltage, respectively, both of which can be nonuniform. Combining and simplifying equations (7) and (8) produces:

$$V_{data} = V_{off} + C\sqrt{I} + D\sqrt[m]{I} \tag{9}$$

where V_{off}, C, and D are combinations of the earlier parameters.

The present invention provides various compensation methods for correcting the intended (input) data voltage V_{data} to compensate for variations in V_{off}, C, D, and m, thereby permitting well-defined OLED currents to be produced in the pixel array. In order to compensate for variations in the parameters V_{off}, C, D, and m, the external current sensing circuits as described above, collect information about each pixel's parameters, i.e., the current drawn by a single pixel can be measured externally. Using the measured information for the parameters V_{off}, C, D, and m, the present invention calculates the appropriate data voltages V_{data} in accordance with equation (9), for establishing the desired OLED currents during normal display operation.

Alternatively, it should be noted that an exact calculation of the four parameters V_{off}, C, D, and m from current measurements is computationally expensive, thereby requiring complicated iterative calculations. However, good approximations can be employed to reduce computational complexity, while maintaining effective compensation.

In one embodiment, pixel nonuniformity is characterized using only two parameters instead of four as discussed above. Referring to the pixel's current-voltage characteristic of equation (9), at normal illumination levels,

the $C\sqrt{I}$ term, associated with V_{gs} of N2, and the $D\sqrt[m]{I}$ term, associated with V_{diode}, have roughly the same magnitude. However, their dependence on pixel current is very different. The value of m is approximately 10, such that at typical illumination levels, $D\sqrt[m]{I}$ is a much weaker function of I than is $C\sqrt{I}$.

For example, a 100 fold (100x) increase in I results in $C\sqrt{I}$ increasing by 10 fold (10x), but $D\sqrt[m]{I}$ increases only 1.58 fold (1.58x) (assuming m = 10). Namely, at typical illumination current levels, the OLED's I-V curve is much steeper than the TFT's I-V_{gs} curve.

As such, an approximation is made where at typical current levels, $D\sqrt[m]{I}$ is independent of current, and its pixel-to-pixel variation can be simply treated as an offset variation. While this approximation may introduce some error, the appearance of the overall display will not be significantly degraded. Thus, with a fair degree of accuracy all display nonuniformity can be treated as offset and gain variations. Thus, equation (9) can be approximated as:

$$V_{data} = V_{offset} + C\sqrt{I} \qquad (10)$$

where $V_{offset} = V_{off} + D\sqrt[m]{I}$ now includes $D\sqrt[m]{I}$, and V_{offset} and C vary from pixel to pixel.

FIG. 14 illustrates a flowchart of a method 1400 for initializing the display by measuring the parameters of all the pixels. Method 1400 starts in step 1405 and proceeds to step 1410, where an "off" data voltage is applied to all pixels in a pixel block, except for the pixel of interest.

In step 1420, to determine V_{offset} and C for a given pixel of interest, method 1400 applies two data voltages (V1 and V2), and the current is measured for each data voltage.

In step 1430, the square root of the currents I1 and I2 are calculated. In one implementation, a square root table is used in this calculation.

In step 1440, V_{offset} and C are determined, i.e., two equations are available to solve two variables. In turn, the calculated V_{offset} and C for a given pixel of interest, are stored in a storage, e.g., memory. After all pixels have been measured, the memory contains the two parameters V_{offset} and C for each pixel in the array. These values can be used at a later time to calibrate or adjust V_{data} in accordance with equation (10). Method 1400 then ends in step 1455.

It should be noted that the current through the measured pixel should be high enough such that $D\sqrt{I}$ can be treated as approximately the same at the two measurement points. Preferably, this condition can be satisfied by making one measurement at the highest data voltage that the system can generate, and then the other measurement at a slightly lower data voltage.

Once display initialization has been performed, the raw input video data supplied to the display module can be corrected. It should be noted that the input video data can exist in various formats, e.g., the video data can represent (1) pixel voltages, (2) gamma-corrected pixel luminances, or (3) pixel currents. As such, the use of the stored parameters V_{offset} and C to calibrate or adjust the input video data depends on each specific format.

FIG. 15 illustrates a flowchart of a method 1500 for correcting input video data representing pixel voltages. Method 1500 starts in step 1505 and proceeds to step 1510, where the stored parameters, e.g., V_{offset} and C are retrieved for a pixel of interest.

In step 1520, method 1500 applies the retrieved parameters to calibrate the input video data. More specifically, it is expected that the input video data are unbiased, i.e., zero volts represents zero luminance, and data greater than zero represent luminance levels greater than zero. Therefore, the voltages can be regarded as equal to $C_0\sqrt{I}$, where I is the desired current and C_0 is a constant, e.g., with a typical value $10^3 V/\sqrt{A}$. To compensate for pixel variations, as input video data enters the display module, the value of $V_{data} = V_{offset} + C\sqrt{I}$ is calculated for each pixel, based on

the stored values of V_{offset} and C. This calculation consists of multiplying the video data by C/C_0, and adding V_{offset} to the result.

The division by C_0 can be avoided if the video data V_{data} has already been scaled by the constant factor $1/C_0$. The multiplication by C can be performed directly in digital logic, or using at look-up table. For example, in the latter case, each value of C specifies a table where the value of the video data is an index, and the table entries consist of the result of the multiplication. (Alternatively, the roles of C and the input video data in the look-up table can be reversed.) After the multiplication is performed, rapid addition of V_{offset} can be implemented with digital logic.

In step 1530, the resulting voltage V_{data}, i.e., the corrected or adjusted input data, is then forwarded to the data driver of pixel array. Method 1500 then ends in step 1535.

In the case of gamma-corrected luminance data, the input video data are proportional to $L^{0.45}$, where L is luminance. This is typical for video data that have been pre-corrected for CRT luminance-voltage characteristics. Since $L^{0.45} \approx \sqrt{L}$, and the OLED luminance is proportional to its current, the data can be treated as proportional to $\sqrt{I}$. Thus, the calculation can be performed in the same way as for zero-offset voltage data as discussed above.

FIG. 16 illustrates a flowchart of a method 1600 for correcting input video data representing pixel currents, i.e., luminances. Method 1600 starts in step 1605 and proceeds to step 1610, where the square-root values of the measured current are calculated. Namely, method 1600 is similar to the method 1500 described above, with the exception that the video data representing I must be processed to yield $\sqrt{I}$. As noted above, this operation can be implemented using a table that provides square-root values as needed for deriving the pixel parameters V_{offset} and C from pixel current measurements, as illustrated in FIG. 14. Here, this table is used again to generate $\sqrt{I}$ from the video data.

Then, the data correction steps 1610-1645 of method 1600 are identical to the method 1500 as described above, with the exception that the

square root of the input data is multiplied by C in step 1630 and then followed by an addition of V_{offset} to yield the corrected data voltage.

Alternatively, in another embodiment, pixel nonuniformity is characterized using only one parameter instead of two or four parameters as discussed above. Namely, an additional simplification is made such that pixel nonuniformity is characterized using a single parameter.

More specifically, in many cases the pixel-to-pixel variation in the gain factor C is small, leaving V_{offset} as the only significant source of nonuniformity. This occurs when the TFT transconductance parameter k and the voltage gain factor B are uniform.. In this case, it is sufficient to determine each pixel's V_{offset}. Then, data correction does not involve multiplication (since the gain factor C is assumed to be uniform), but only involves addition of the offset parameter.

This one-parameter approximation is similar to the above autozeroing OLED pixel structures. The present one-parameter compensation method should produce satisfactory display uniformity, while reducing computational expense. However, if maintaining display uniformity is very important to a particular display application, then the above described two or four-parameter methods can be employed at the expense of increasing computational complexity and expense.

Again, for one-parameter extraction and data correction, the display initialization process depends on the format of the data. The single-parameter method can be used to initialize the display and to correct video data for the cases of video data representing (1) pixel voltages, (2) pixel currents, and (3) gamma-corrected pixel luminances.

FIG. 17 illustrates a flowchart of a method 1700 for initializing the display by measuring the parameters of all the pixels. Method 1700 starts in step 1705 and proceeds to step 1710, where an "off" data voltage is applied to all pixels in a pixel block, except for the pixel of interest.

In step 1720, to determine V_{offset} and C for a given pixel of interest, method 1700 applies two data voltages (V1 and V2), and the current is measured for each data voltage.

In step 1730, the square root of the currents I1 and I2 are calculated. In one implementation, a square root table is used in this calculation.

It should be noted that since the value of C is supposed to be uniform, then ideally it can be determined by making a two-point measurement on a single pixel anywhere in the display. However, this is questionable, since the pixel of interest may be unusual. Thus, a two-point measurement is made on every pixel.

In step 1740, the average C is determined. Namely, using a table to calculate $\sqrt{I}$ for each current measurement, an average value of C for the display can be calculated.

In step 1750, V_{offset} is determined for each pixel from its current measurements based on the average C. In this manner, small variations in C across the display are partially compensated by the calculated V_{offset}. For reasons given above, it is preferable to make each pixel's current measurement at the highest possible data voltage.

Finally, in step 1760, each pixel's V_{offset} is stored in a storage, e.g., memory. Method 1700 then ends in step 1765.

FIG. 18 illustrates a flowchart of a method 1800 for correcting input video data representing pixel voltages. Method 1800 starts in step 1805 and proceeds to step 1810, where the stored parameters, e.g., V_{offset} is retrieved for a pixel of interest.

In step 1820, method 1800 applies the retrieved parameter V_{offset} to calibrate the input video data. More specifically, the value of $V_{data} = V_{offset} + V_{data}$ is calculated for each pixel, based on the stored value of V_{offset}.

In step 1830, the resulting voltage V_{data}, i.e., the corrected or adjusted input data, is then forwarded to the data driver of pixel array. Method 1800 then ends in step 1835.

FIG. 19 illustrates a flowchart of a method 1900 for initializing the display by measuring the parameters of all the pixels for the situation where the video data represents pixel currents. It should be noted that

method 1900 is very similar to method 1700 as discussed above. The exception arises when method 1900 incorporates an additional step 1950, where a calculated average value of C is used to generate a table of zero-offset data voltage vs. pixel current. From this point forward in the initialization and data correction processes, square root operations can be avoided by using this table. The table is expected to provide a more accurate representation of the pixel's current-voltage characteristics than the square-root function. The table is then stored in a storage, e.g., a memory for later use. Then the individual pixel current measurements are used as indexes to enter this table, and individual pixel offsets V_{offset} are determined.

FIG. 20 illustrates a flowchart of a method 2000 for correcting input video data represented in pixel currents, i.e., luminances. Method 2000 starts in step 2005 and proceeds to step 2010, where the current pixel of interest's V_{offset} is retrieved from storage.

In step 2020, the zero-offset data voltage vs. pixel current table is used to obtain a zero-offset data voltage from the input video data current. This zero-offset data voltage is added to the retrieved V_{offset} in step 2030. Finally, in step 2040, the corrected or adjusted input video data, is then forwarded to the data driver of the pixel array.

In sum, as video data are introduced into the display module, the zero-offset data voltage corresponding to each current is looked up in the V-I table. Then the stored pixel offset is added to the zero-offset voltage, and the result is the input to the data driver. Method 2000 then ends in step 2045.

FIG. 21 illustrates a flowchart of a method 2100 for initializing the display by measuring the parameters of all the pixels for the situation where the video data represents gamma-corrected luminance data. It should be noted that method 2100 is very similar to method 1900 as discussed above. The exception arises in step 2150 of method 2100, where a calculated average value of C is used to generate a table of zero-offset data voltage vs. the square root of the pixel current. Namely, the video data can

be approximated as representing $\sqrt{I}$. As such, the average value of C is used to create a zero-offset table of V_{data} vs. $\sqrt{I}$, and this table is saved in a storage such as a memory.

FIG. 22 illustrates a flowchart of a method 2200 for correcting input video data represented in gamma-corrected luminance data. It should be noted that method 2200 is very similar to method 2000 as discussed above. The only exception arises in the zero-offset table of V_{data} vs. $\sqrt{I}$. Thus, in sum, incoming video data are used to look up the zero-offset data voltages, and stored pixel offsets are added to these voltages.

It should be noted that the above description assumes that the OLED drive transistor N2 is operated in saturation. Similar compensation methods can be used, if N2 is operated in the linear region. In that case, the pixel's current voltage characteristic is expressed as:

$$V_{data} = V_{off} + C(I)I + D\sqrt{I} \quad (11)$$

where C(I) is a weak function of I. Again, the $D\sqrt{I}$ term can be incorporated in V_{off}, if the current is sufficiently high, such that only an offset term and a gain factor need to be determined as discussed above. However, the one-parameter approximation, where only the offset voltage is regarded as nonuniform, is not anticipated to be as accurate as the above one-parameter approximation for the saturation case, because now the gain factor C(I) contains the nonuniform OLED parameters A and m. Thus, the two-parameter correction method will likely perform significantly better than the one-parameter correction method, if N2 is operated in the linear region.

FIG. 23 illustrates a block diagram of a system 2300 employing a display 2320 having a plurality of active matrix LED pixel structures 300, 500, or 700 of the present invention. The system 2300 comprises a display controller 2310 and a display 2320.

More specifically, the display controller can be implemented as a general purpose computer having a central processing unit CPU 2312, a

memory 2314 and a plurality of I/O devices 2316 (e.g., a mouse, a keyboard, storage devices, e.g., magnetic and optical drives, a modem, A/D converter, various modules, e.g., measurement module 1330 as discussed above, and the like). Software instructions (e.g., the various methods described above) for activating the display 2320 can be loaded, e.g., from a storage medium, into the memory 2314 and executed by the CPU 2312. As such, the software instructions of the present invention can be stored on a computer-readable medium.

The display 2320 comprises a pixel interface 2322 and a plurality of pixels (pixel structures 300, 500, or 700). The pixel interface 2322 contains the necessary circuitry to drive the pixels 300, 500, or 700. For example, the pixel interface 2322 can be a matrix addressing interface as illustrated in FIG. 1 and may optionally include additional signal/control lines as discussed above.

Thus, the system 2300 can be implemented as a laptop computer. Alternatively, the display controller 2310 can be implemented in other manners such as a microcontroller or application specific integrated circuit (ASIC) or a combination of hardware and software instructions. In sum, the system 2300 can be implemented within a larger system that incorporates a display of the present invention.

Although the present invention is described using NMOS transistors, it should be understood that the present invention can be implemented using PMOS transistors, where the relevant voltages are reversed.

Although various embodiments which incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

What is claimed is:

1. A display comprising at least one pixel, said pixel comprising:

a first transistor having a gate, a source and a drain, where said gate is for coupling to a first select line;

a capacitor having a first and second terminals, where said drain of said first transistor is coupled to said first terminal of said capacitor;

a second transistor having a gate, a source and a drain, where said drain of said first transistor is coupled to said drain of said second transistor, where said gate of said second transistor is for coupling to an autozero line;

a third transistor having a gate, a source and a drain, where said source of said third transistor is coupled to said drain of said second transistor, where said gate of said third transistor is for coupling to a second select line;

a fourth transistor having a gate, a source and a drain, where said drain of said fourth transistor is coupled to said source of said second transistor, where said gate of said fourth transistor is coupled to said source of said first transistor;

a fifth transistor having a gate, a source and a drain, where said drain of said fifth transistor is coupled to said drain of said third transistor, where said gate of said fifth transistor is coupled to said source of said first transistor; and

a light element having two terminals, where said source of said fourth transistor and said source of said fifth transistor are coupled to one of said terminal of said light element.

2. The display of claim 1, wherein said light element is an organic light emitting diode (OLED).

3. The display of claim 1, wherein said transistors are thin film transistors constructed from amorphous-silicon.

4. The display of claim 1, wherein said second select line is an autozero line from a previous row.

5. A display comprising at least one pixel, said pixel comprising:

a first transistor having a gate, a source and a drain, where said gate is for coupling to a select line;

a capacitor having a first and second terminals, where said drain of said first transistor is coupled to said first terminal of said capacitor;

a second transistor having a gate, a source and a drain, where said drain of said first transistor is coupled to said drain of said second transistor, where said gate of said second transistor is for coupling to an autozero line;

a diode having a first and second terminals, where said source of said second transistor is coupled to said first terminal of said diode, where said second terminal of said diode is for coupling to an illuminate line;

a third transistor having a gate, a source and a drain, where said drain of said third transistor is coupled to said first terminal of said diode, where said gate of said third transistor is coupled to said source of said first transistor; and

a light element having two terminals, where said source of said third transistor is coupled to one of said terminal of said light element.

6. The display of claim 5, wherein said diode is a Schottky diode.

7. A display comprising at least one pixel, said pixel comprising:

a first transistor having a gate, a source and a drain, where said gate is for coupling to a first select line;

a capacitor having a first and second terminals, where said drain of said first transistor is coupled to said first terminal of said capacitor;

a second transistor having a gate, a source and a drain, where said source of said first transistor is coupled to said source of said second

transistor, where said gate of said second transistor is for coupling to an autozero line;

a third transistor having a gate, a source and a drain, where said source of said third transistor is coupled to said drain of said second transistor, where said gate of said third transistor is for coupling to a second select line;

a fourth transistor having a gate, a source and a drain, where said drain of said fourth transistor is coupled to said source of said third transistor, where said gate of said fourth transistor is coupled to said source of said first transistor;

a fifth transistor having a gate, a source and a drain, where said drain of said fifth transistor is coupled to said drain of said third transistor, where said gate of said fifth transistor is coupled to said source of said first transistor; and

a light element having two terminals, where said source of said fourth transistor and said source of said fifth transistor are coupled to one of said terminal of said light element.

8. The display of claim 7, wherein said light element is an organic light emitting diode (OLED).

9. The display of claim 7, wherein said second select line is an autozero line from a previous row.

10. A display comprising:

at least one autozeroing pixel structure;

an autozero line, coupled to said autozeroing pixel structure, for allowing said autozeroing pixel structure to perform autozeroing; and

a second line, coupled to said autozeroing pixel structure, for carrying a voltage to said autozeroing pixel structure that permits a range of autozero voltages to be extended.

11. A method of illuminating a display having at least one pixel, where said pixel contains a circuit for controlling application of energy to a light element, said method comprising the steps of:

(a) autozeroing the pixel;

(b) loading data onto said pixel via a data line; and

(c) illuminating said light element in accordance with said stored data.

12. The method of claim 11, further comprising the step of:

(a') precharging said pixel prior to said autozeroing step (a).

13. The method of claim 11, wherein said autozeroing step (a) comprises the step of applying a reference black level.

14. A method of illuminating a display having at least one pixel, said method comprising the steps of:

(a) measuring a pixel parameter of said pixel;

(b) adjusting an input pixel data in accordance with said measured pixel parameter; and

(c) illuminating said pixel in accordance with said adjusted input pixel data.

15. The method of claim 14, wherein said measuring step (a) measures externally a current drawn by said pixel.

16. The method of claim 15, wherein said adjusting step (b) adjusts said pixel data by using said measured pixel parameter to determine a voltage offset (V_{offset}) parameter.

17. The method of claim 16, wherein said adjusting step (b) further adjusts said pixel data by using said measured pixel parameter to determine a gain factor (C) parameter.

18. A system comprising:

a display controller; and

a display, coupled to said display controller, where said display comprises a plurality of pixels, where each pixel comprises:

a first transistor having a gate, a source and a drain, where said gate is for coupling to a first select line;

a capacitor having a first and second terminals, where said drain of said first transistor is coupled to said first terminal of said capacitor;

a second transistor having a gate, a source and a drain, where said source of said first transistor is coupled to said source of said second transistor, where said gate of said second transistor is for coupling to an autozero line;

a third transistor having a gate, a source and a drain, where said source of said third transistor is coupled to said drain of said second transistor, where said gate of said third transistor is for coupling to a second select line;

a fourth transistor having a gate, a source and a drain, where said drain of said fourth transistor is coupled to said source of said third transistor, where said gate of said fourth transistor is coupled to said source of said first transistor;

a fifth transistor having a gate, a source and a drain, where said drain of said fifth transistor is coupled to said drain of said third transistor, where said gate of said fifth transistor is coupled to said source of said first transistor; and

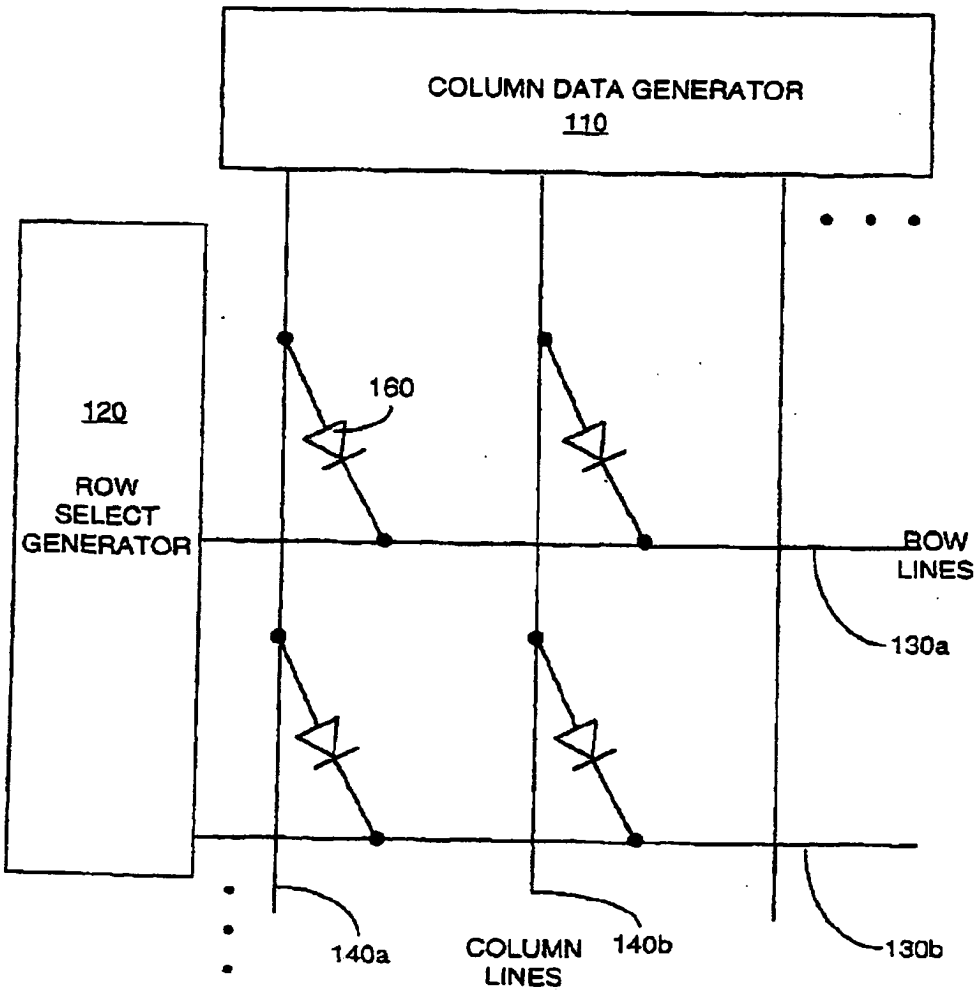
a light element having two terminals, where said source of said fourth transistor and said source of said fifth transistor are coupled to one of said terminal of said light element.

19. A system comprising:

a display controller having a measurement module for measuring a pixel parameter of a pixel and a storage for storing said measured pixel parameter; and

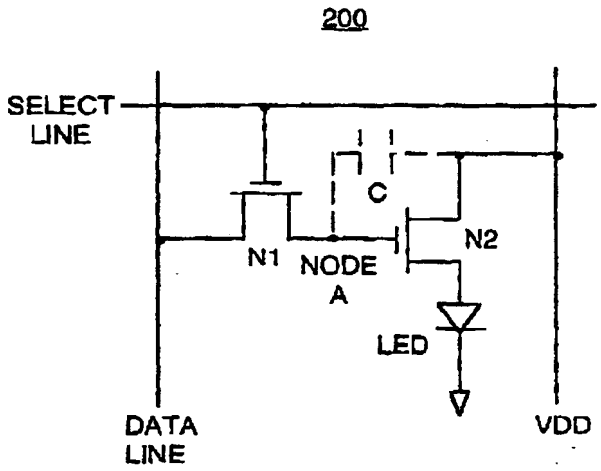
a display, coupled to said display controller, for displaying an input pixel data that is adjusted in accordance with said stored pixel parameter.

20. The system of claim 19, wherein said measurement module comprises a current sensing circuit for measuring a current drawn by said pixel.



(PRIOR ART)

FIG. 1



(PRIOR ART)

FIG. 2

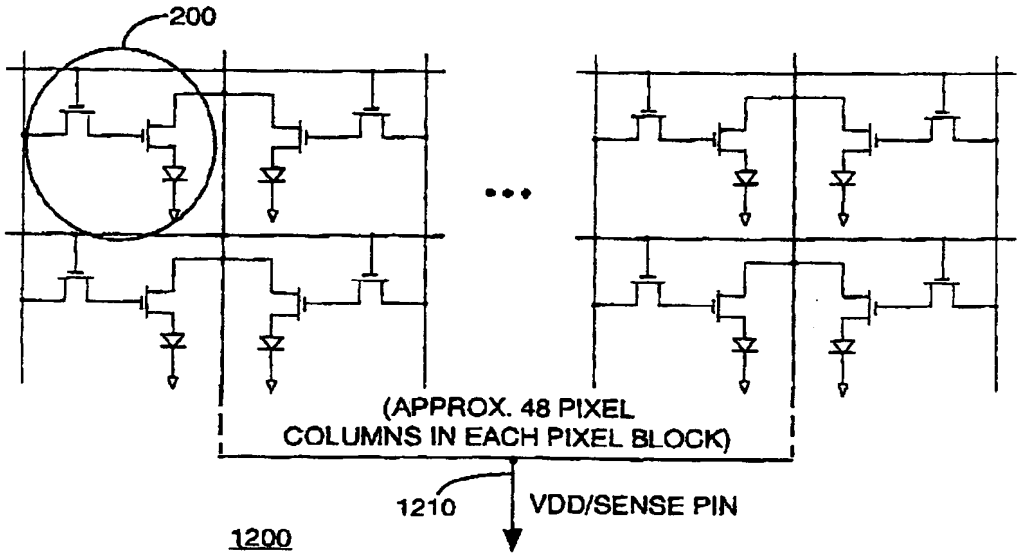


FIG. 12

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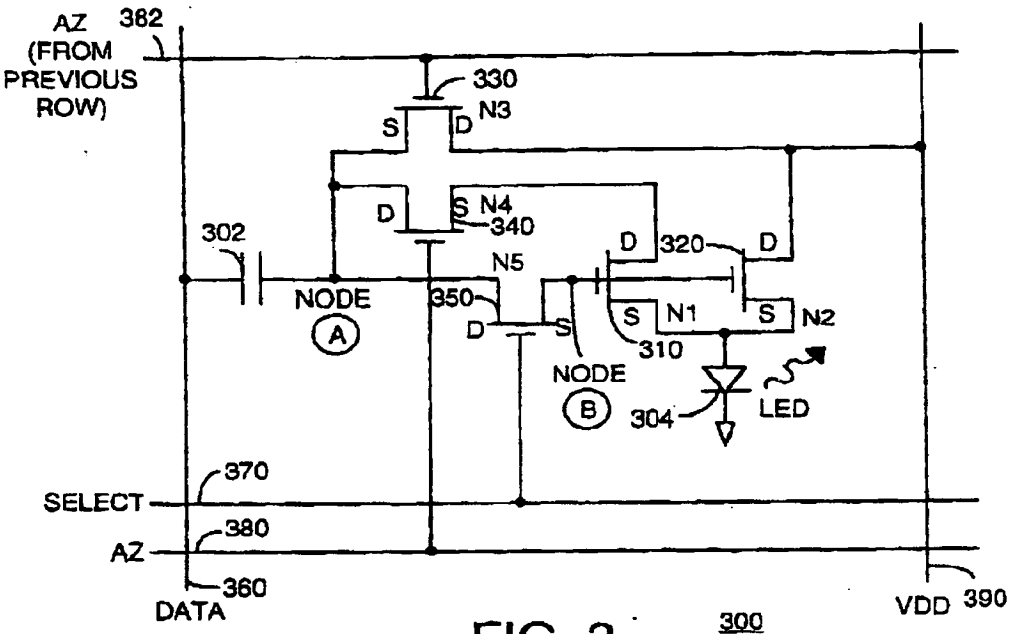

FIG. 3

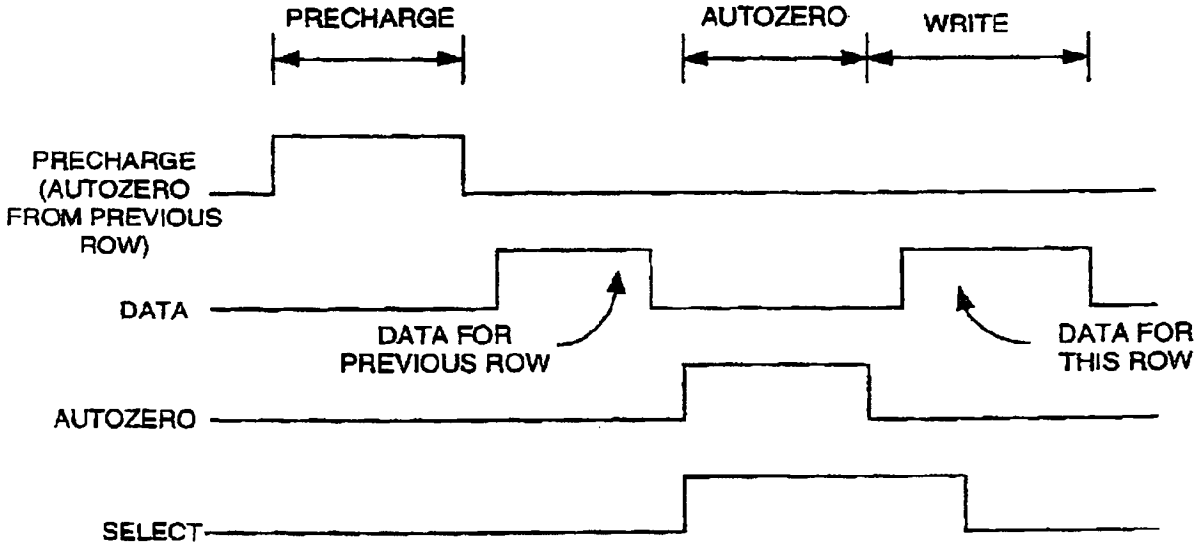

FIG. 4

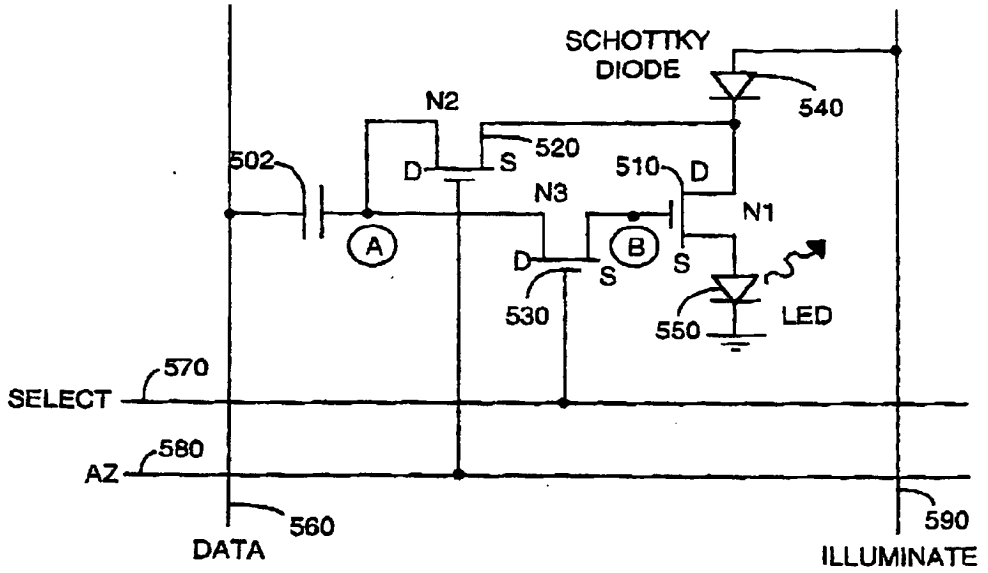

FIG. 5 500

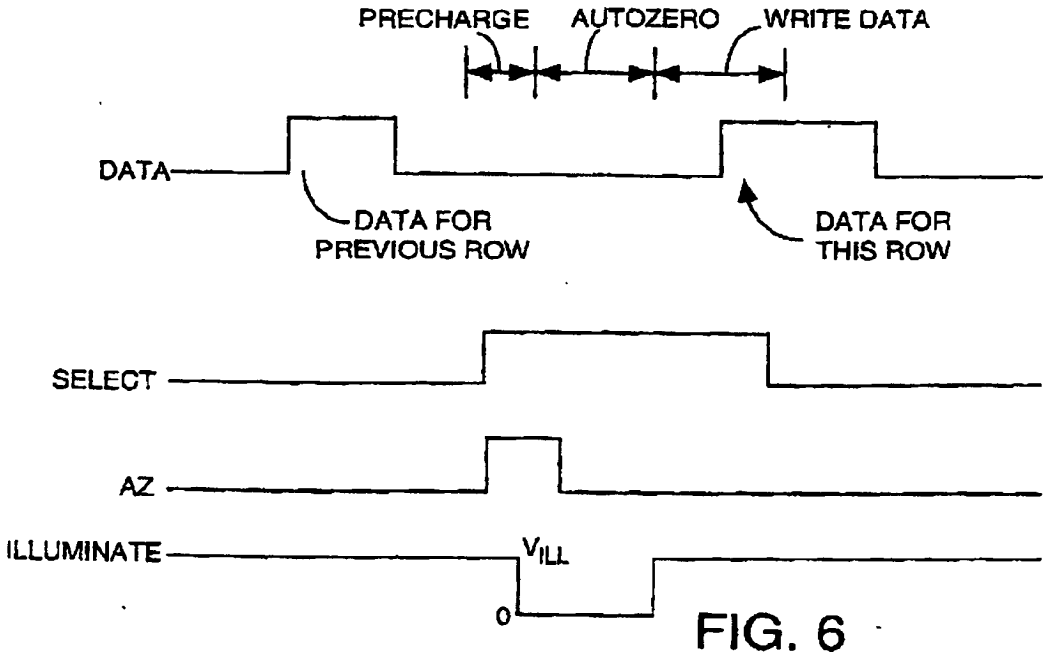

FIG. 6

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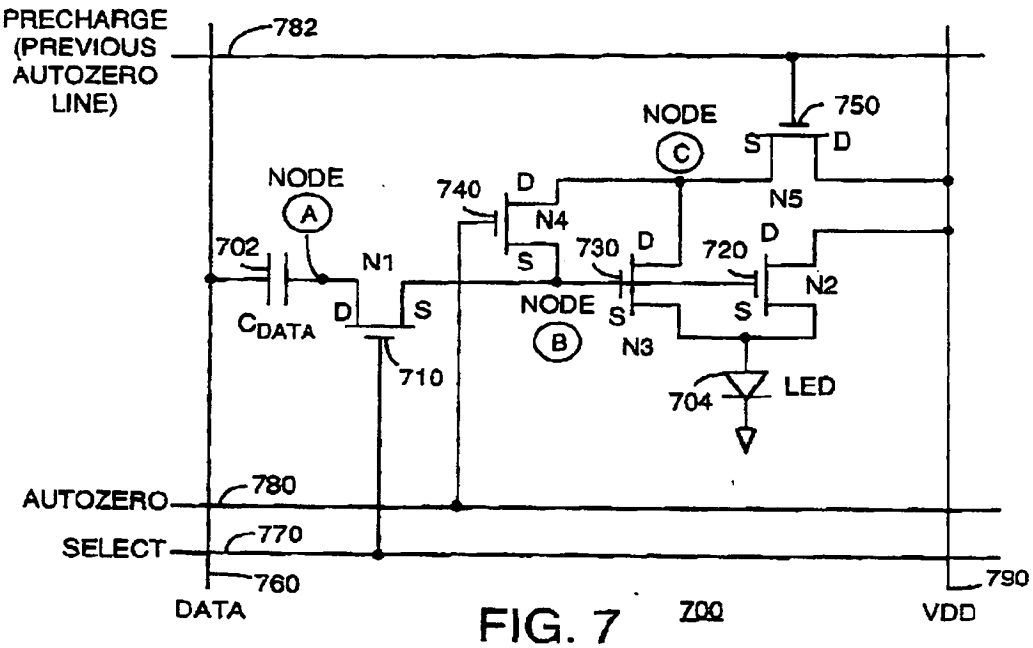

FIG. 7

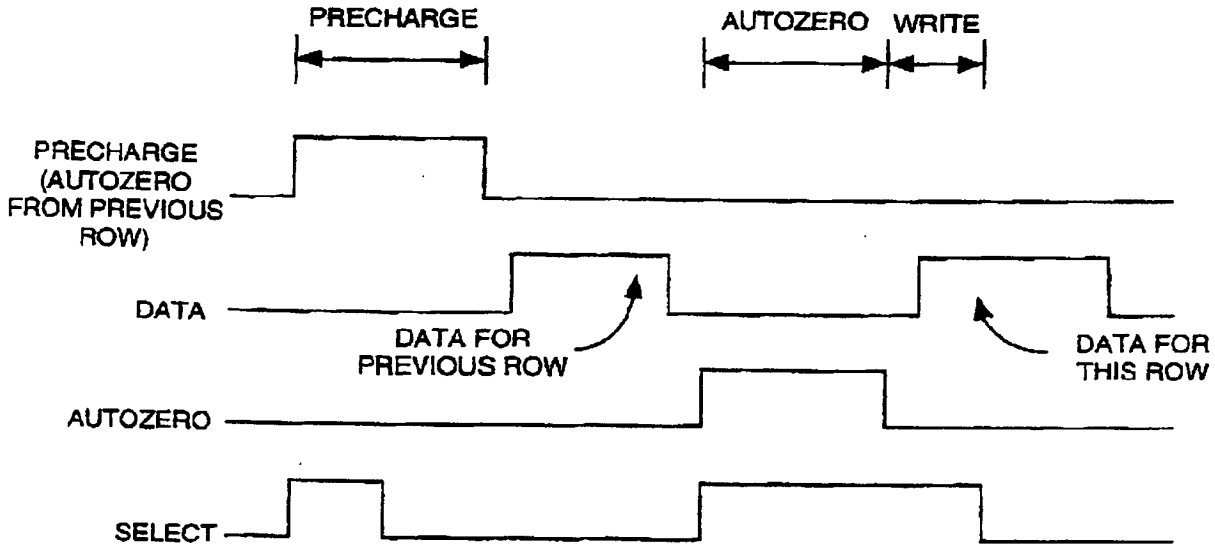

FIG. 8

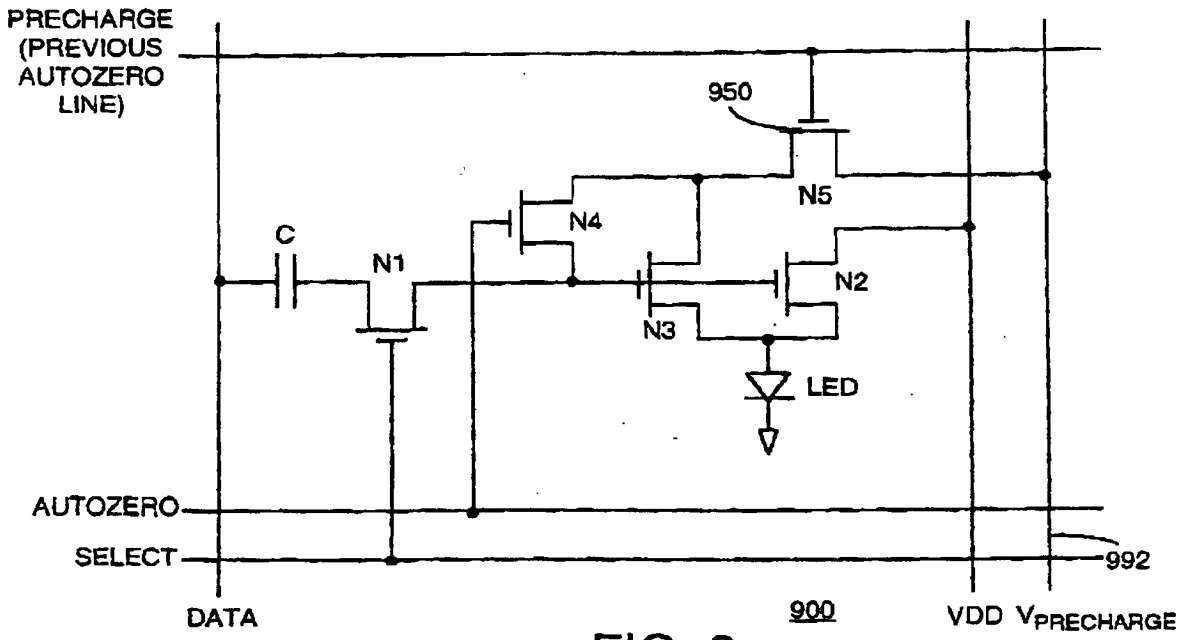
PRECHARGE
(PREVIOUS
AUTOZERO
LINE)
950
N5
N4
C
N1
N2
N3
LED
AUTOZERO
SELECT
992
DATA
900
VDD
VPRECHARGE

FIG. 9

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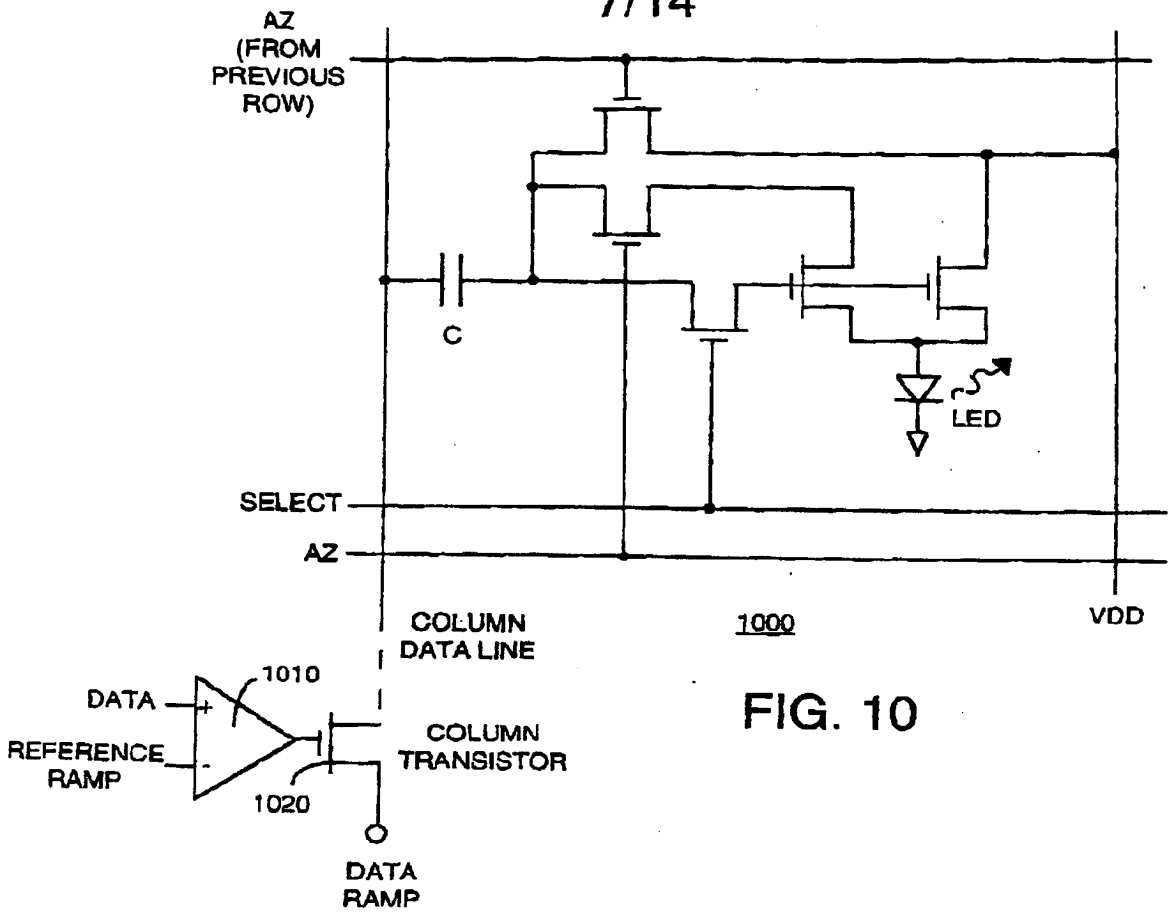

FIG. 10

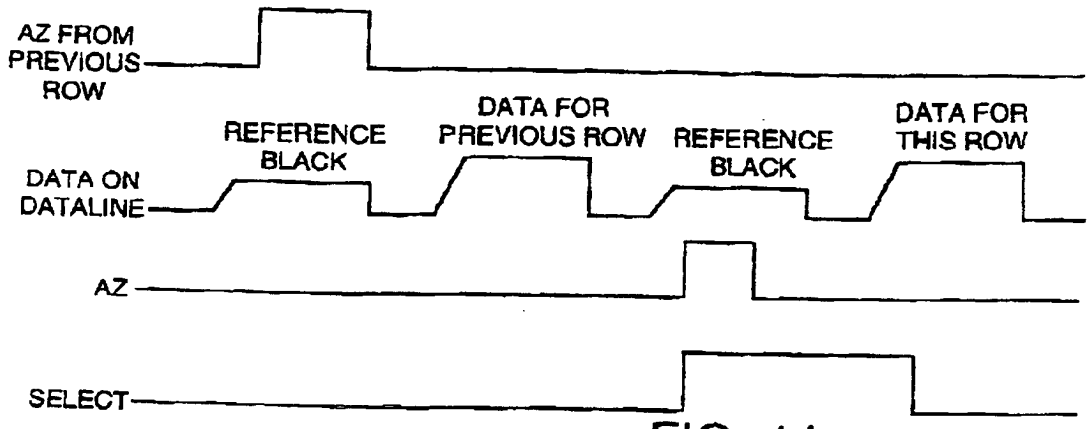

FIG. 11

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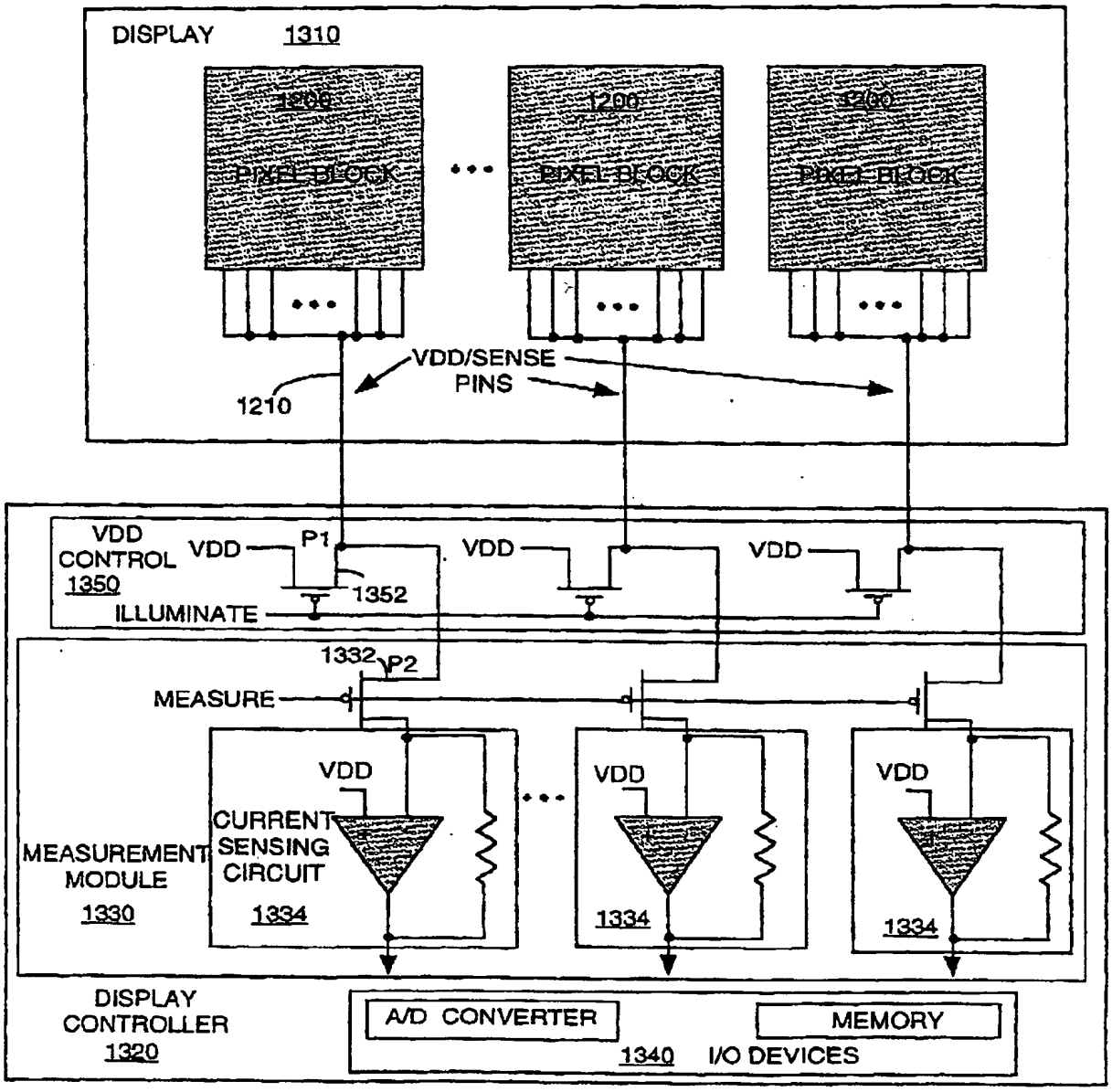
DISPLAY 1310
1200
PIXEL BLOCK
1200
PIXEL BLOCK
1200
PIXEL BLOCK
VDD/SENSE PINS
1210
VDD CONTROL 1350
VDD
P1
1352
ILLUMINATE
VDD
VDD
1332
P2
MEASURE
VDD
VDD
VDD
CURRENT SENSING CIRCUIT 1334
MEASUREMENT MODULE 1330
1334
1334
DISPLAY CONTROLLER 1320
A/D CONVERTER
MEMORY
1340 I/O DEVICES

FIG. 13

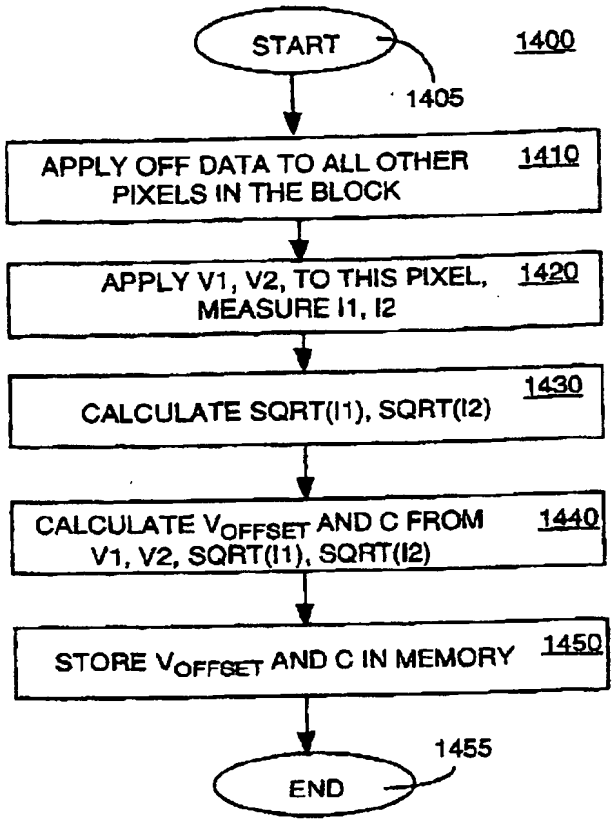
START
1400
1405
APPLY OFF DATA TO ALL OTHER PIXELS IN THE BLOCK
1410
APPLY V1, V2, TO THIS PIXEL, MEASURE I1, I2
1420
CALCULATE SQRT(I1), SQRT(I2)
1430
CALCULATE V_{OFFSET} AND C FROM V1, V2, SQRT(I1), SQRT(I2)
1440
STORE V_{OFFSET} AND C IN MEMORY
1450
1455
END

FIG. 14

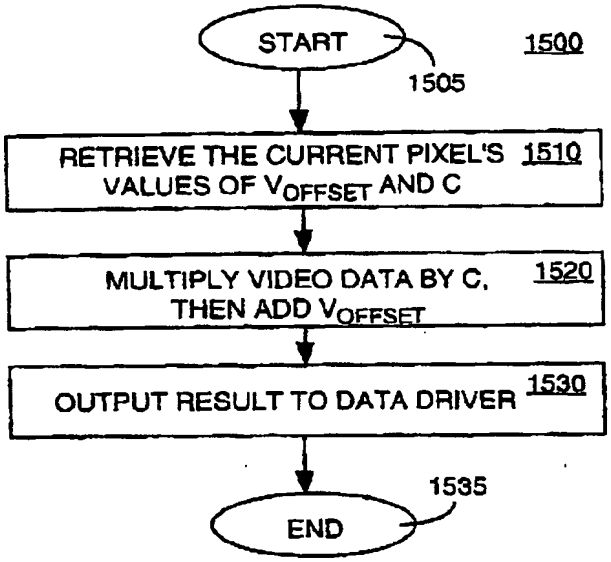
START
1500
1505
RETRIEVE THE CURRENT PIXEL'S VALUES OF V_{OFFSET} AND C
1510
MULTIPLY VIDEO DATA BY C, THEN ADD V_{OFFSET}
1520
OUTPUT RESULT TO DATA DRIVER
1530
1535
END

FIG. 15

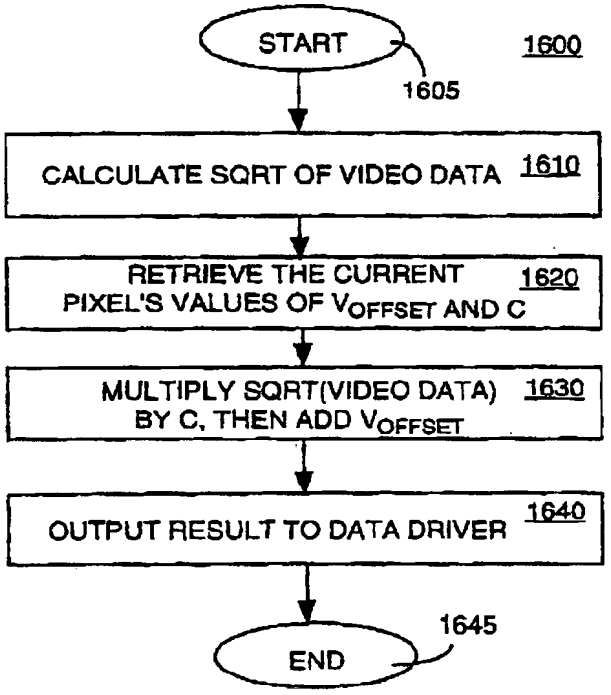
START
1600
1605
CALCULATE SQRT OF VIDEO DATA
1610
RETRIEVE THE CURRENT PIXEL'S VALUES OF V_{OFFSET} AND C
1620
MULTIPLY SQRT(VIDEO DATA) BY C, THEN ADD V_{OFFSET}
1630
OUTPUT RESULT TO DATA DRIVER
1640
1645
END

FIG. 16

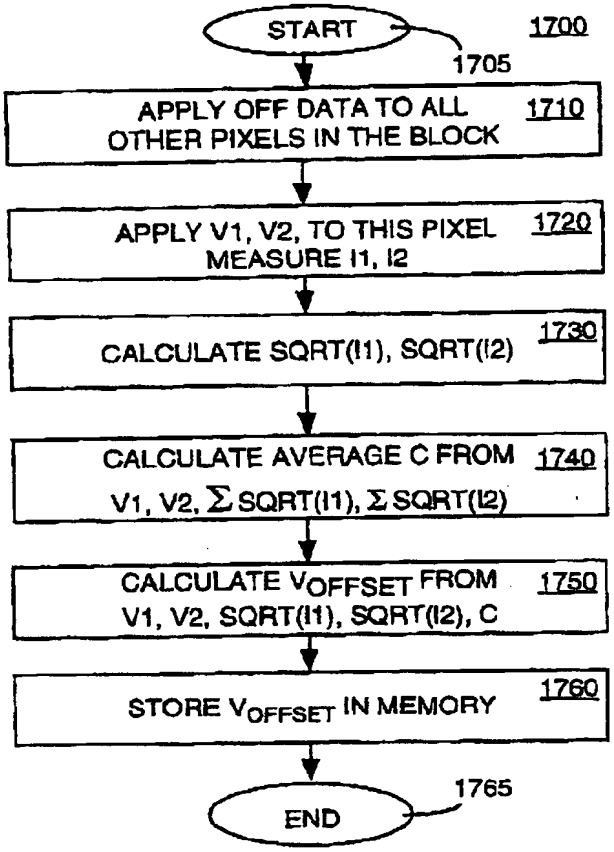
START
1700
1705
APPLY OFF DATA TO ALL OTHER PIXELS IN THE BLOCK
1710
APPLY V1, V2, TO THIS PIXEL MEASURE I1, I2
1720
CALCULATE SQRT(I1), SQRT(I2)
1730
CALCULATE AVERAGE C FROM V1, V2, Σ SQRT(I1), Σ SQRT(I2)
1740
CALCULATE V_{OFFSET} FROM V1, V2, SQRT(I1), SQRT(I2), C
1750
STORE V_{OFFSET} IN MEMORY
1760
END
1765

FIG. 17

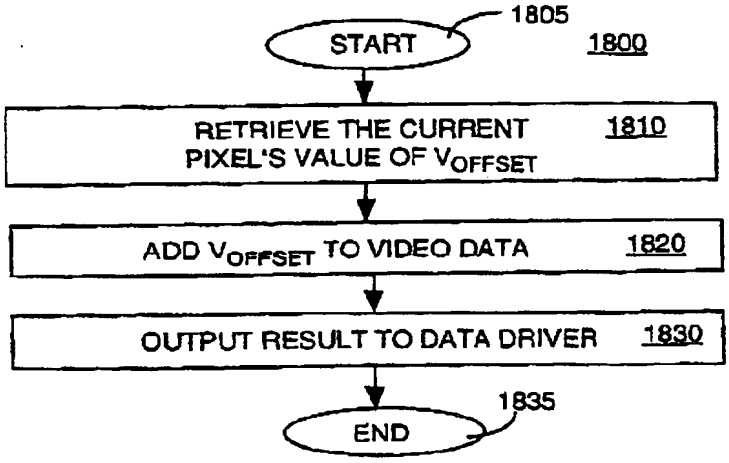
START
1805
1800
RETRIEVE THE CURRENT PIXEL'S VALUE OF V_{OFFSET}
1810
ADD V_{OFFSET} TO VIDEO DATA
1820
OUTPUT RESULT TO DATA DRIVER
1830
END
1835

FIG. 18

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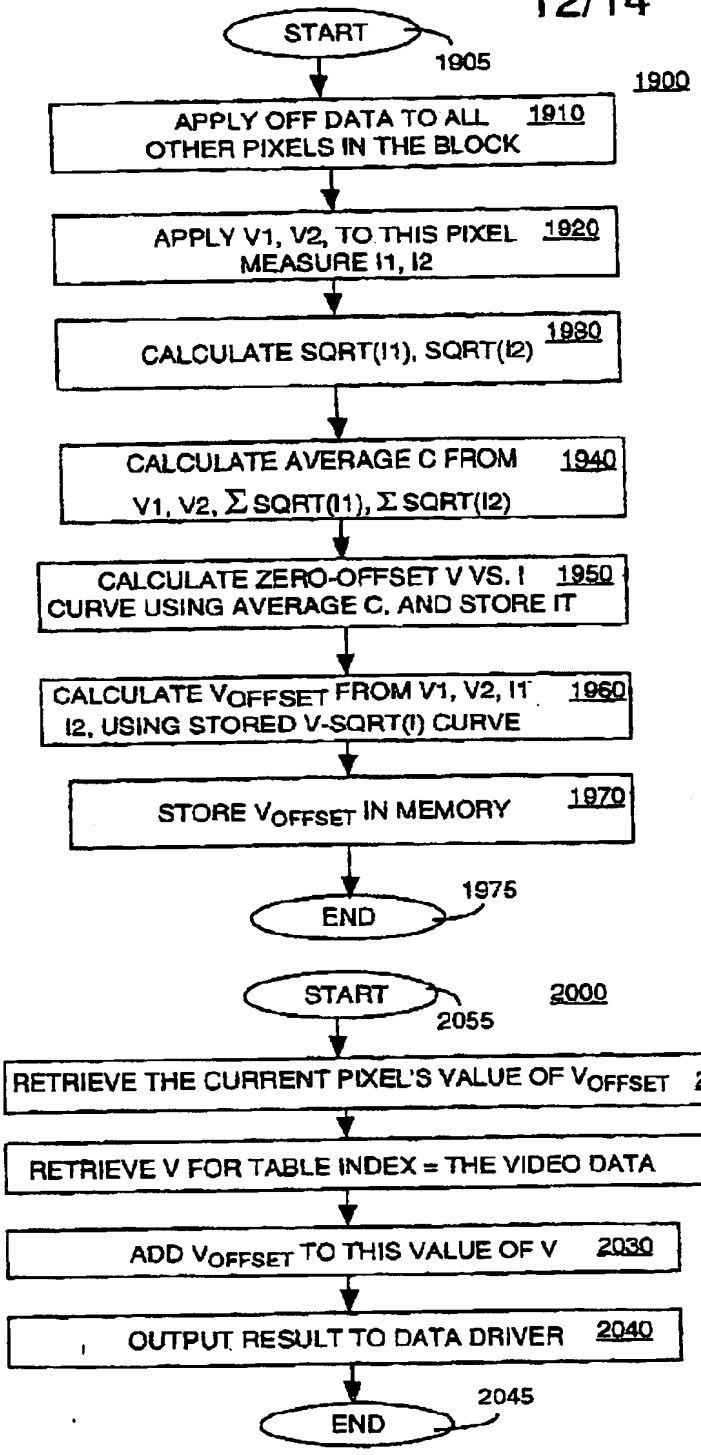

FIG. 19

FIG. 20

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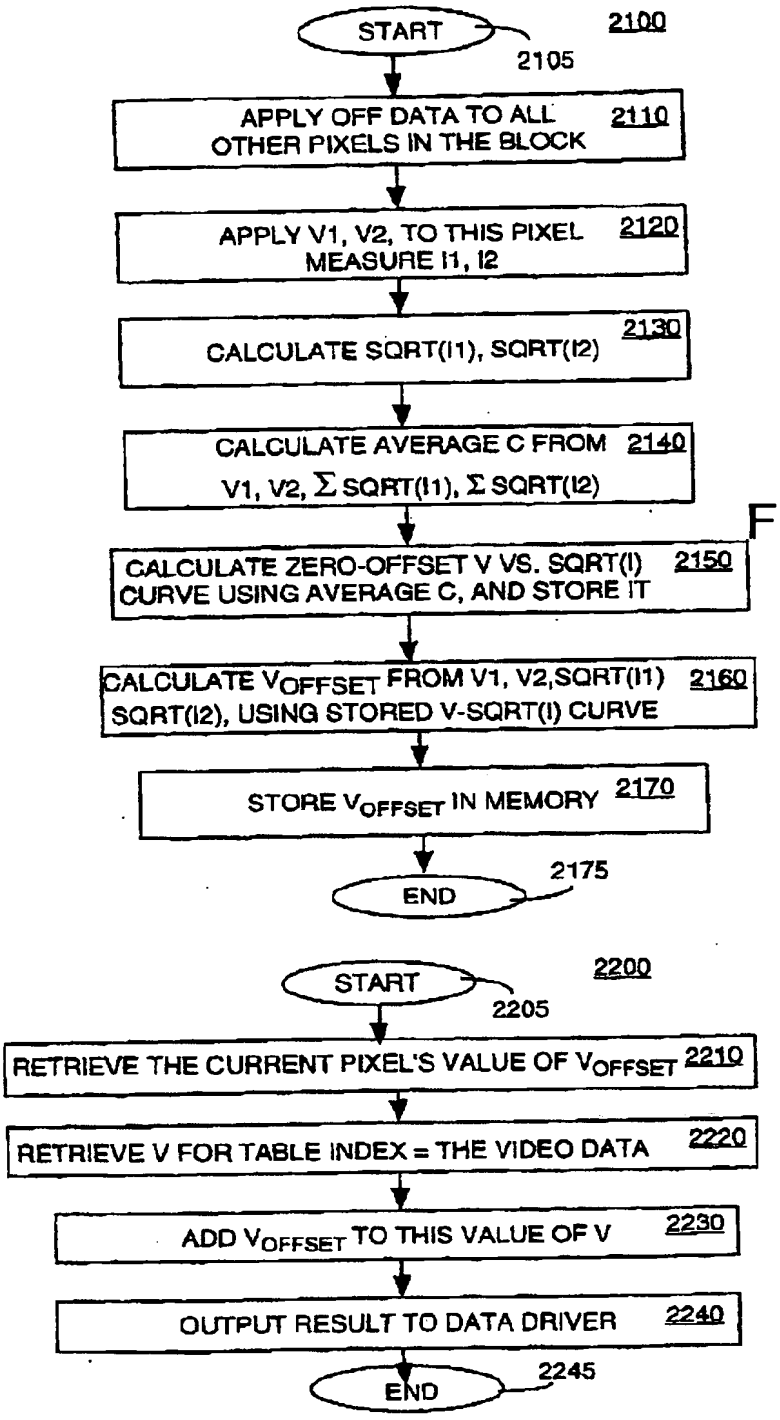

FIG. 21

FIG. 22

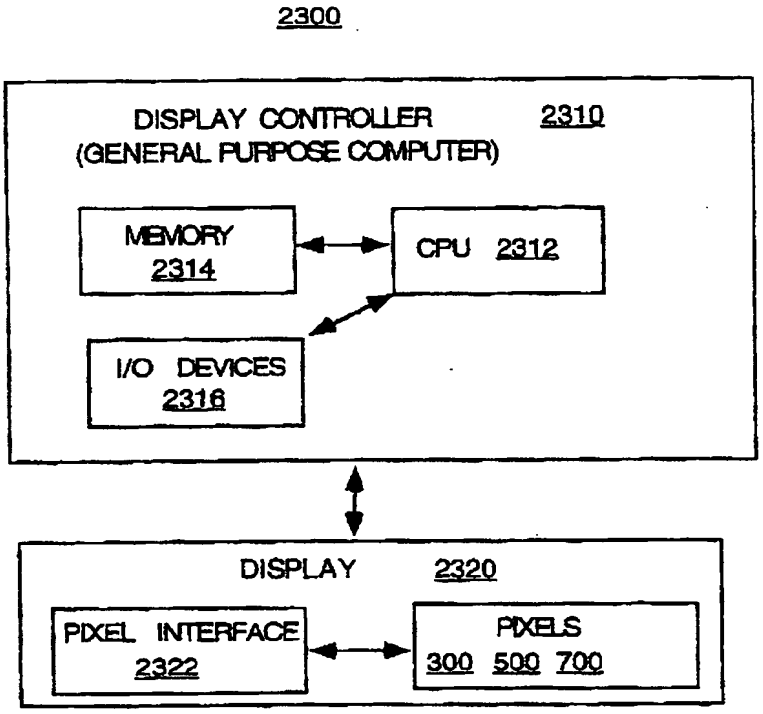
2300
DISPLAY CONTROLLER
(GENERAL PURPOSE COMPUTER)
2310
MEMORY
2314
CPU 2312
I/O DEVICES
2316
DISPLAY
2320
PIXEL INTERFACE
2322
PIXELS
300 500 700

FIG. 23

Abstract of the Disclosure

LED pixel structures and methods that improve brightness uniformity by reducing current nonuniformities in a light-emitting diode of the pixel structures are disclosed.

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